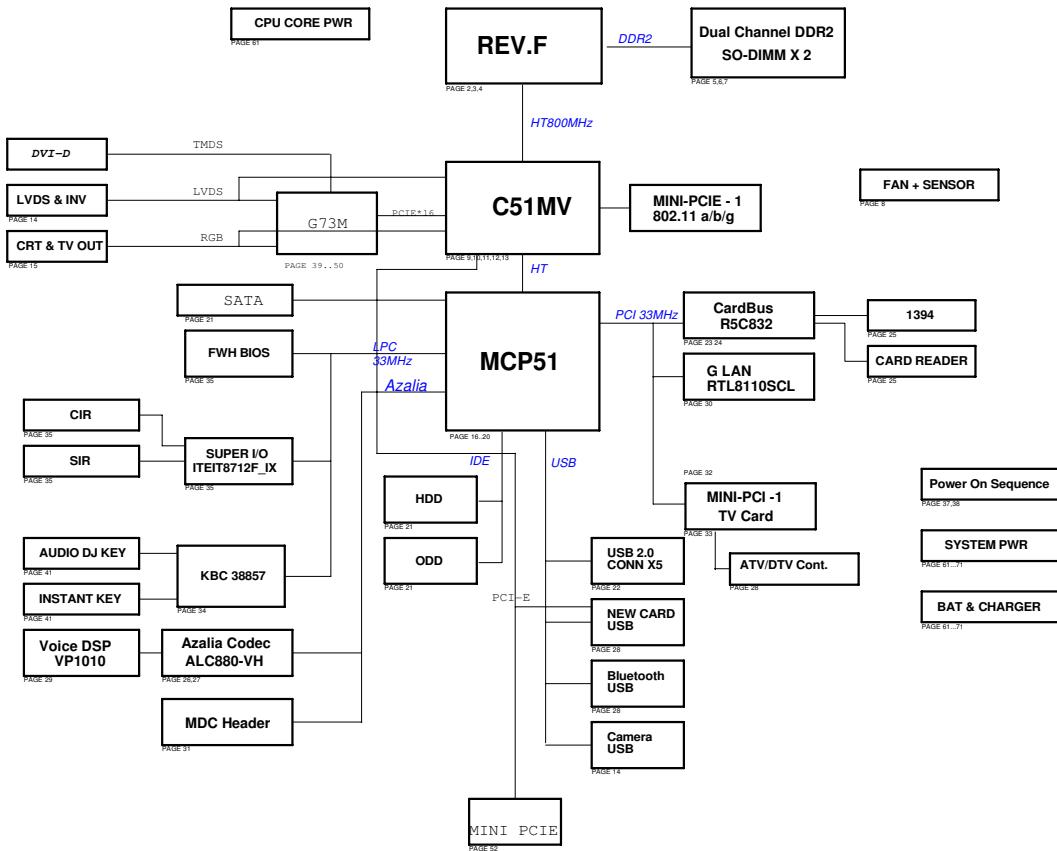
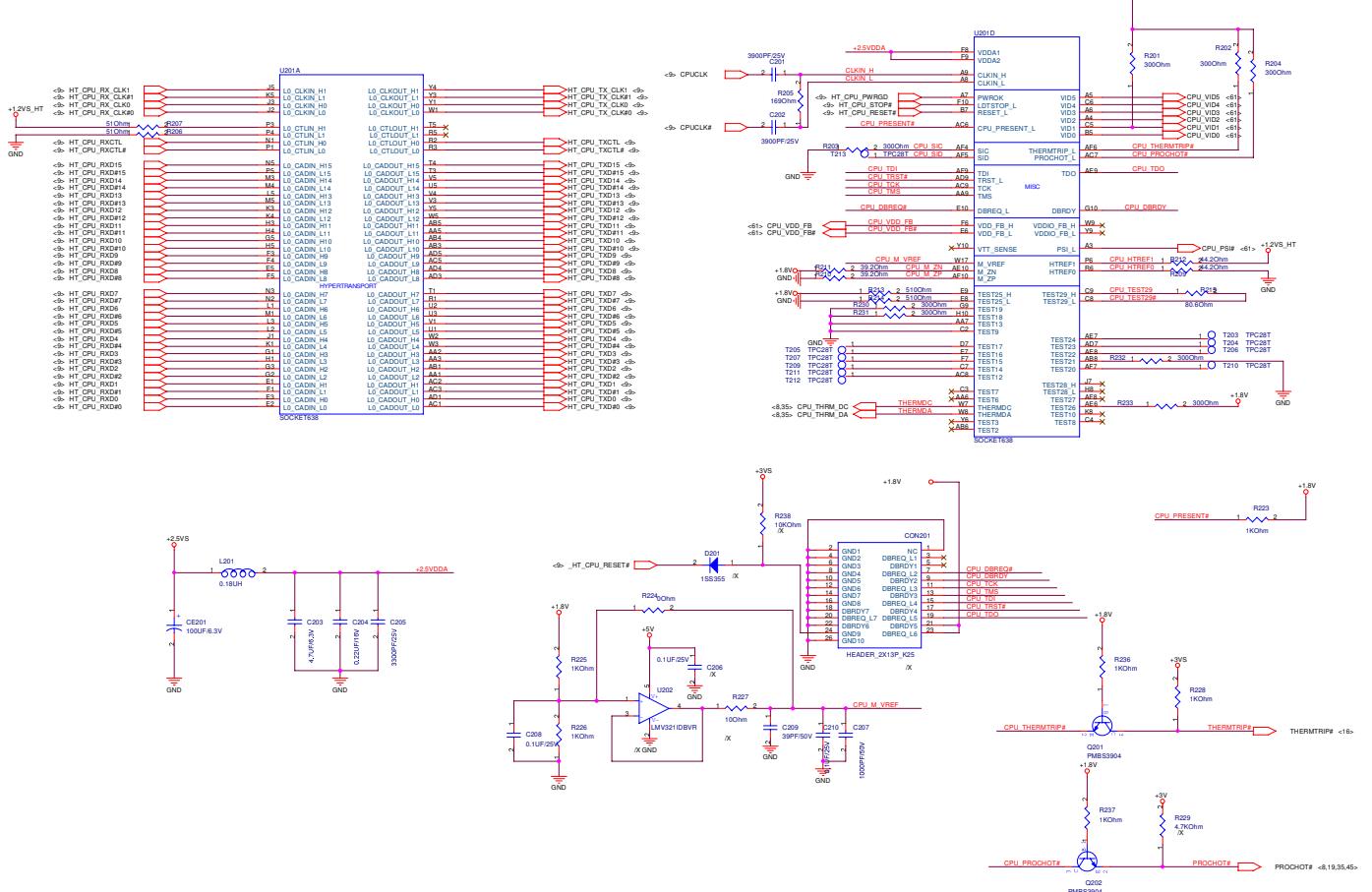


# A7T/M BLOCK DIAGRAM

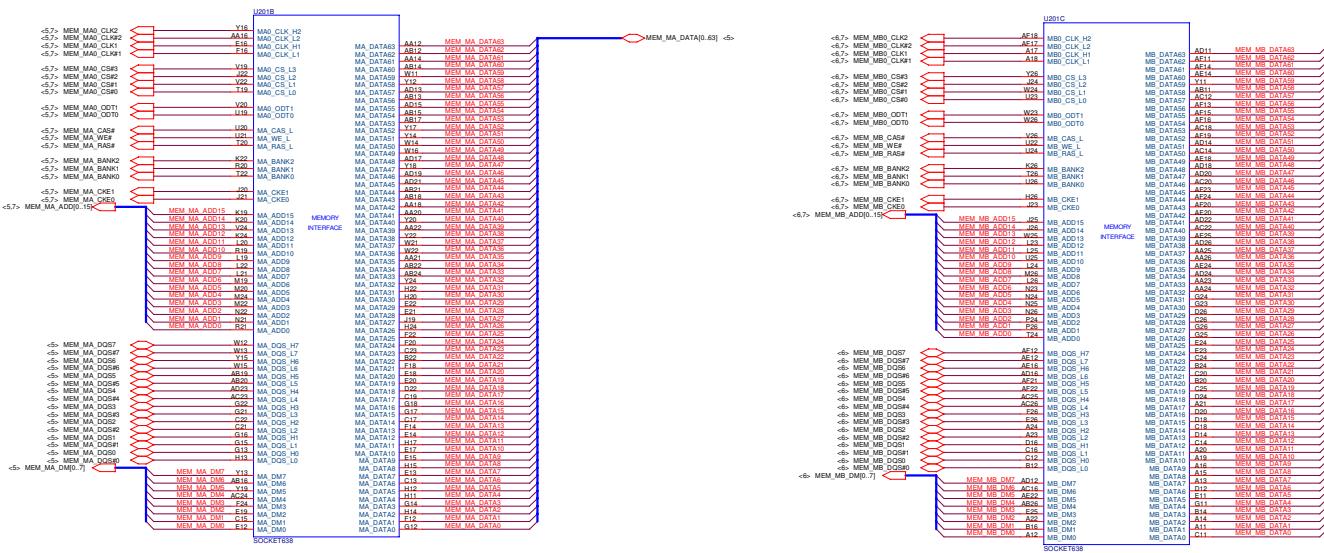


01_BLOCK DIAGRAM	41_G73M_PCIEX16_1
02_AMD S1 CPU(1)	42_G73M_PCIEX16_2
03_AMD S1 CPU(2)	43_G73M_DISPLAY
04_AMD S1 CPU(3)	44_G73M_BIOS&CRY
05_DDR2_SO_DIMM-1	45_G73M_GPIO
06_DDR2_SO_DIMM-2	46_G73M_STRAP
07_DDR2_SODIMMS	47_G73M_VRAM1
08_THERMAL&FAN	48_G73M_VRAM2
09_C51M_HT_CPU	49_G73M_VRAM3
10_C51M_HT_MCP	50_G73M_VRAM4
11_C51M_PCIEx16	51_RJ11+45&MINI
12_C51M_VGA_OUTPUT	52_NEWCARD (802.11)
13_C51M_POWER&GND	61_Vcore
14_LVDS CONNECTER	62_SYSTEM
15_CRT_TV_CONNECTER	63_1.2VO&+1.8VO
16_MCP51_HT_I/F	64_2.5V & 0.9V_3VA
17_MCP51_PCI_I/F	65_VGACORE
18_MCP51_IDE	66_1V_C51_CORE
19_MCP51_USB	67_LOAD SWITCH
20_MCP51_POWER	68_CHARGE
21_HDD&ODD	69_PIC16C54
22_USB	70_BATCONN
23_CARDBUS RSC841	71_PWRGD_SHUTDOWN#
24_CARDBUS SOCKET	53_SYSTEM RESOURCE
25_1394 CON	54_HISTORY
26_ALC880	
27_AMP	
28_BT/FR/RF	
29_VOICE DSP	
30_LAN_RTL8100TL	
31_RJ11+45&MDC	
32_MINIPCI (802.11)	
33_MINIPCI (TV)	
34_KBC 38857	
35_SUPER I/O	
36_FUNCTION KEY	
37_PWR ON SEQ-1	
38_PWR ON SEQ-2	
39_G73M_FB_1	
40_G73M_FB_2	

<< Kennedy\_Zhang >>

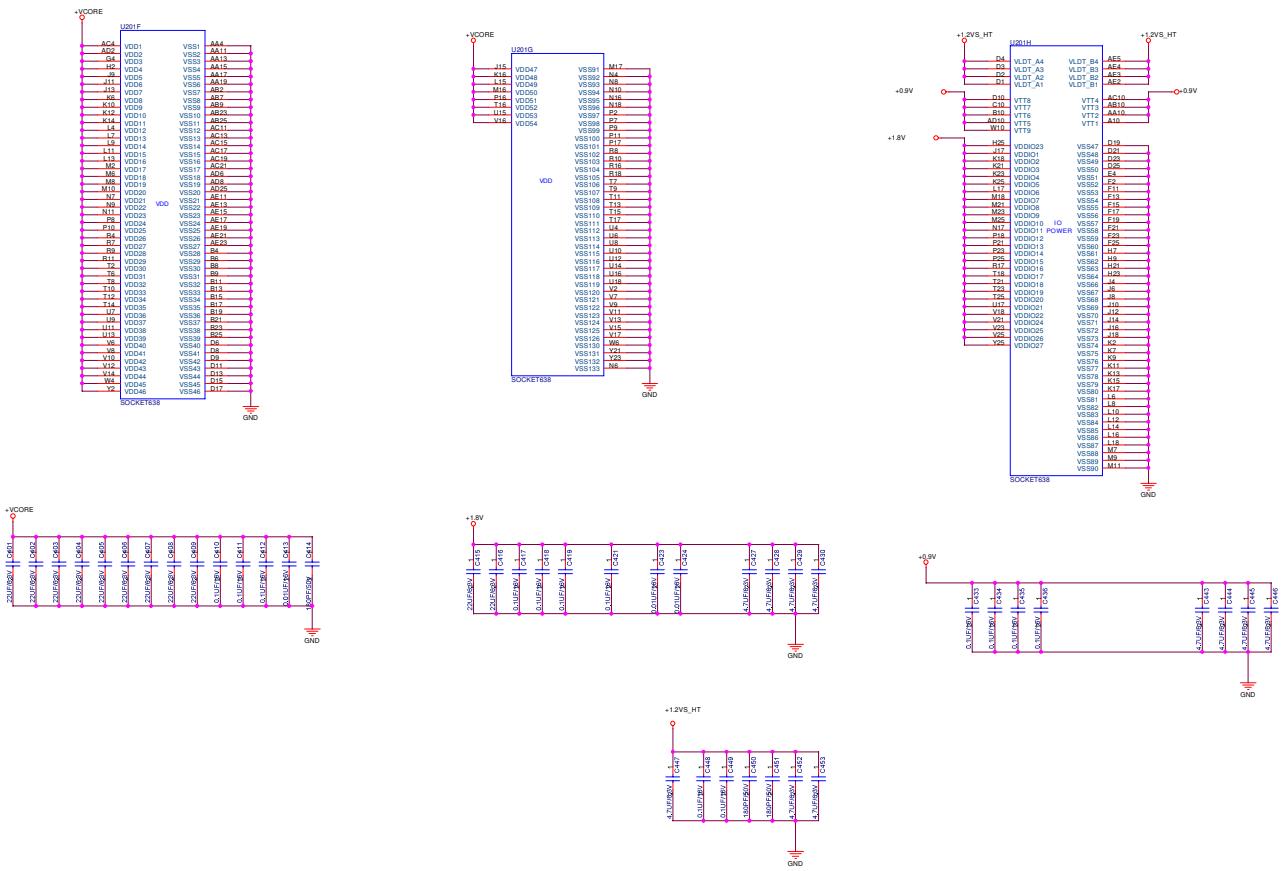


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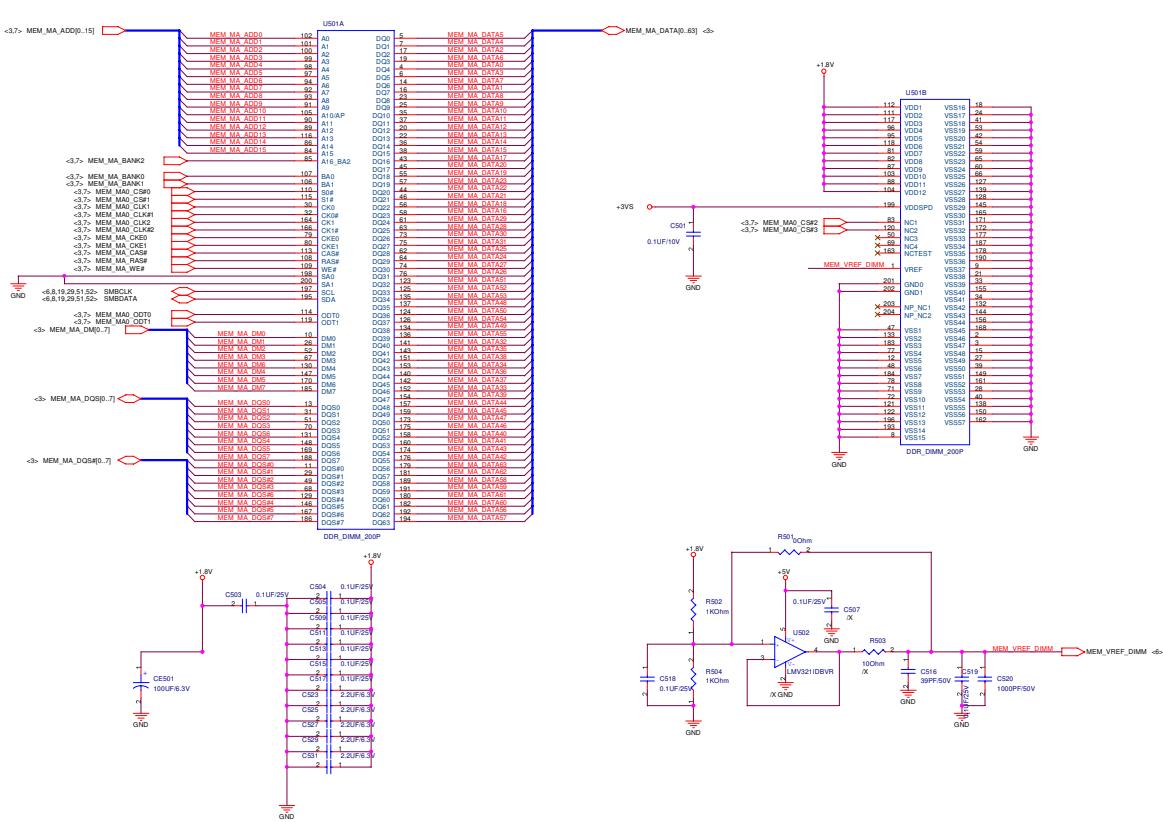
<< Kennedy\_Zhang >>

ASUSTECH  
Engineer: Heby\_wang  
Size Project Name Rev  
C A7T 2.0  
Date: 2006-08-02 Sheet 3 of 73



**ASUS** Title : AMD S1 CPU(3)  
 ASUSTECH Engineer: Heby\_wang  
 Size: C Project Name: ATT Rev: 2.0  
 Date: 01/28/2006 Sheet: 4 of 73

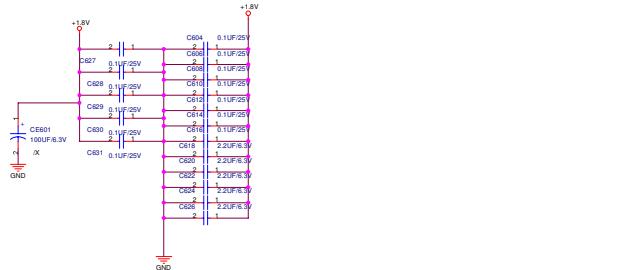
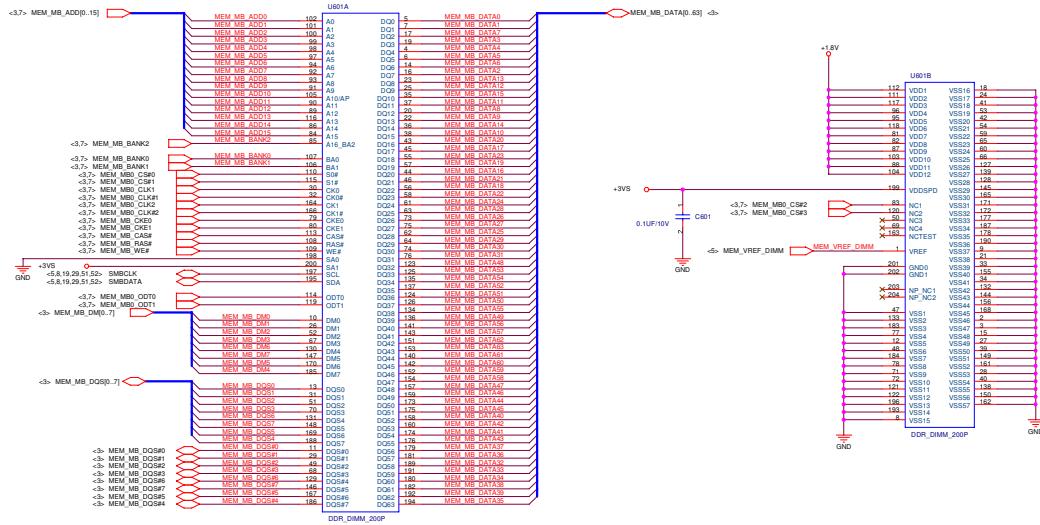
<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>

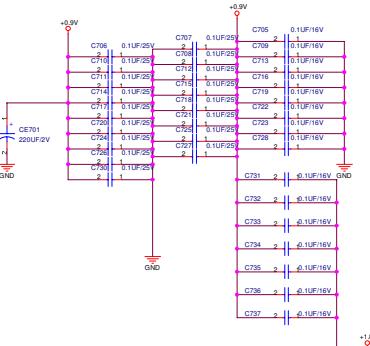
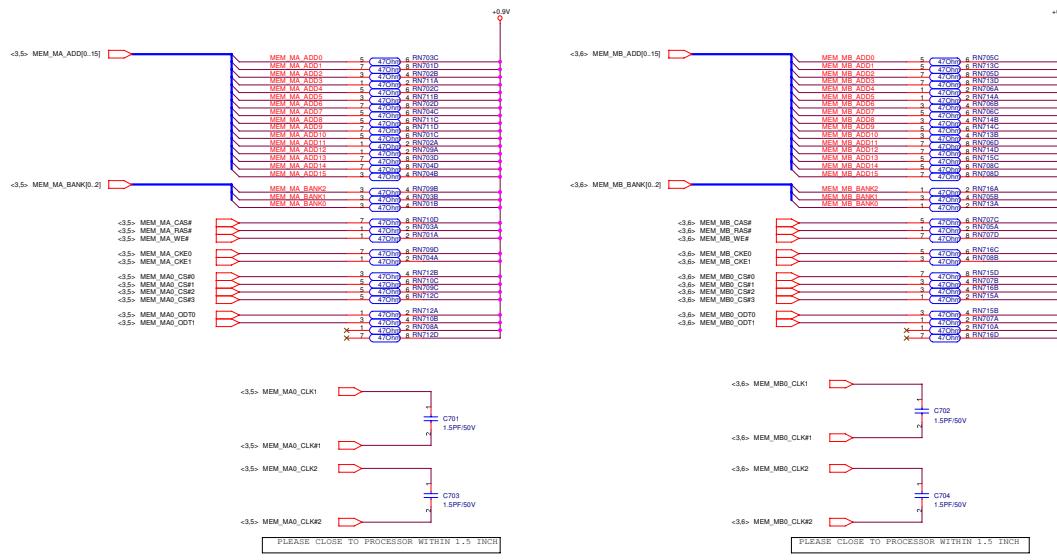
**ASUS** Title : DDR2\_SO\_DIMM(0)  
 ASUSTECH Engineer: *Heby\_wang*  
 Size Project Name Rev  
 C A7T 2.0  
 Date: 2006-02-02 Sheet 5 of 73

## BOTTOM



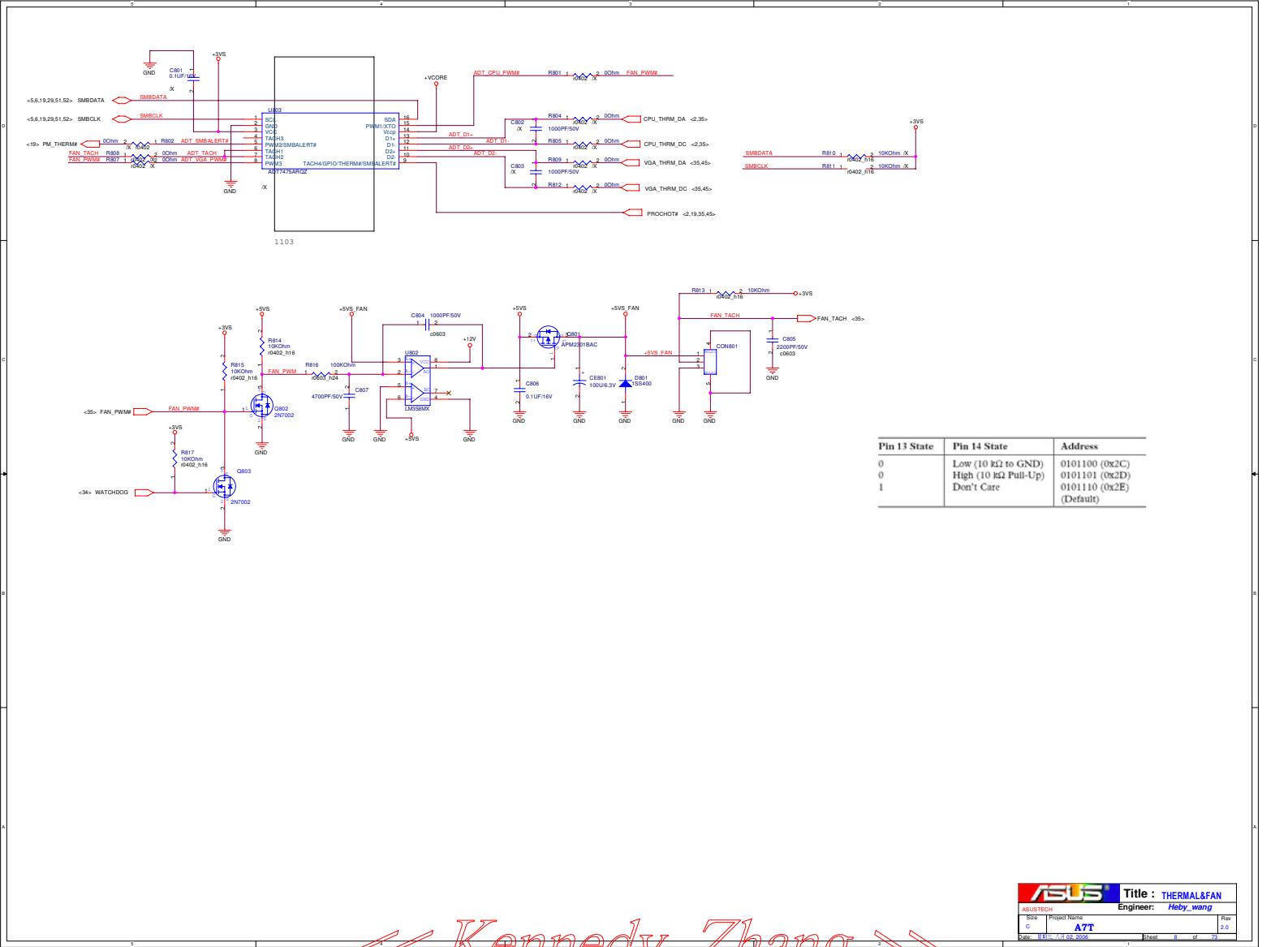
<< Kennedy\_Zhang >>

ASUS Title : DDR2\_SO\_DIMM(1)  
 ASUSTECH Engineer: Heby\_wang  
 Size Project Name Rev  
 C A7T 2.0  
 Date: 8/16, 2006 Sheet 6 of 73

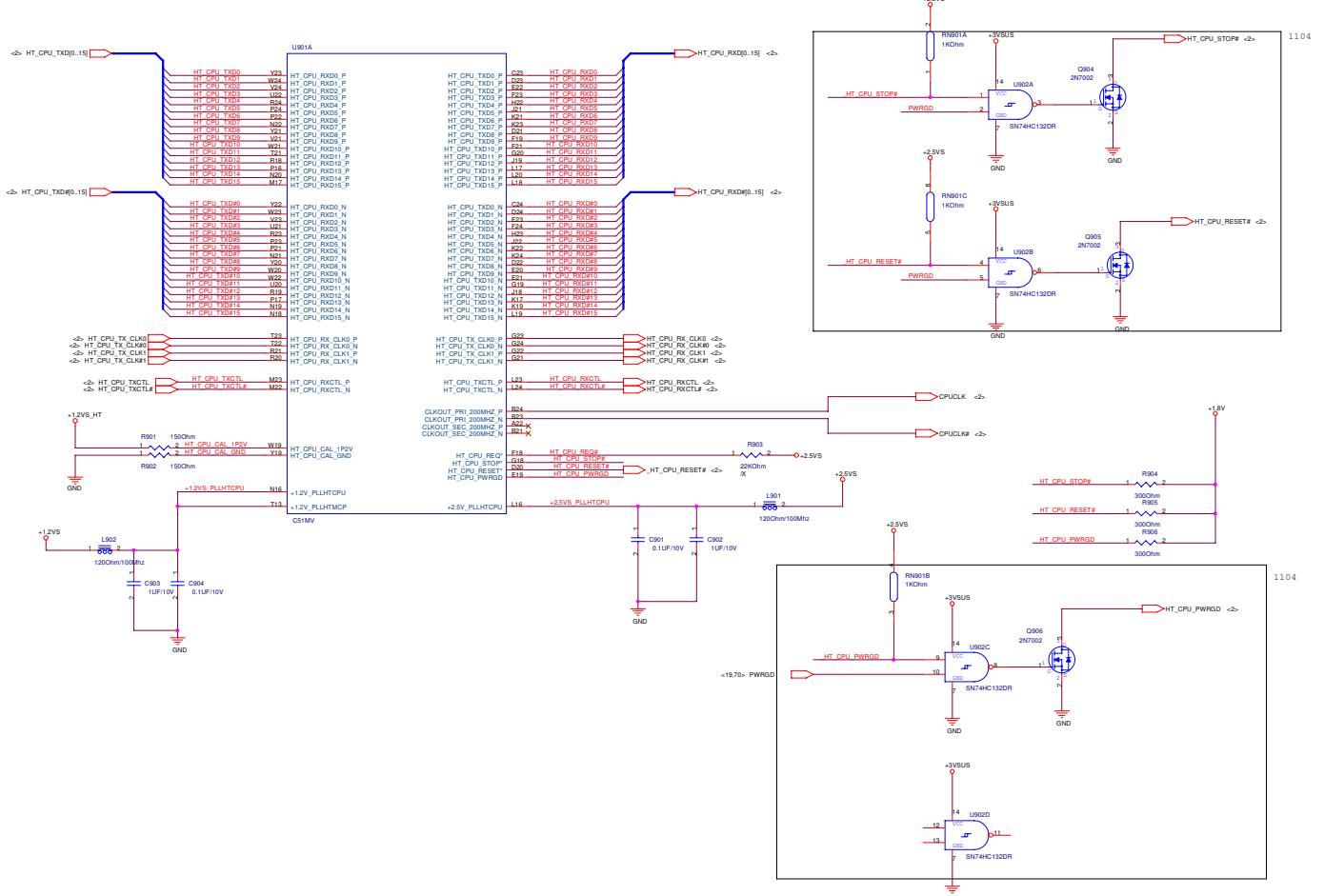


**ASUS Title : DDR2TERMINATIONS**  
**ASUSTECH Engineer: Heby\_wang**  
**Size: C Project Name: ATT Rev: 2.0**  
**Date: Feb. 01 28 2006 Sheet: 7 of 73**

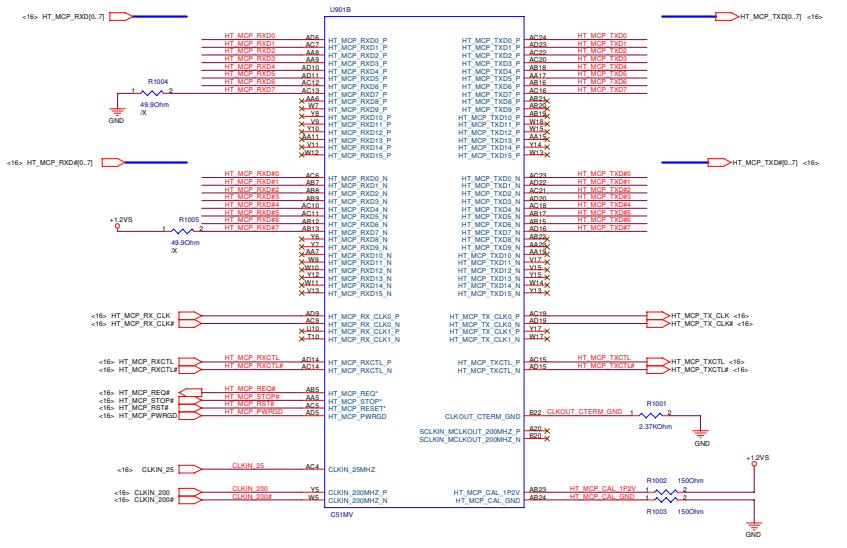
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<< Kennedy\_Zhang >>

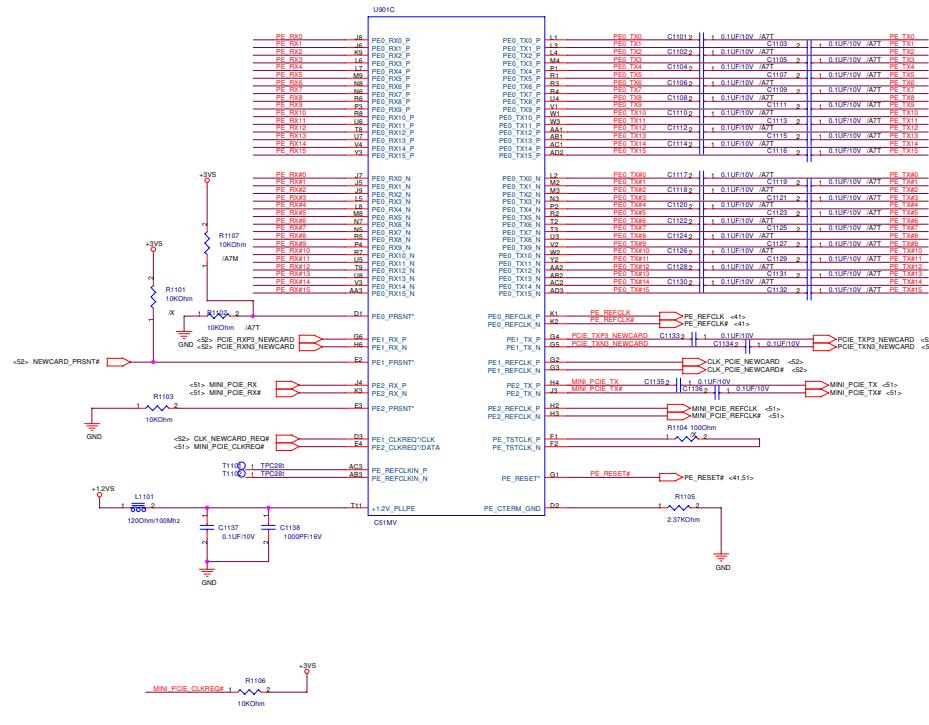


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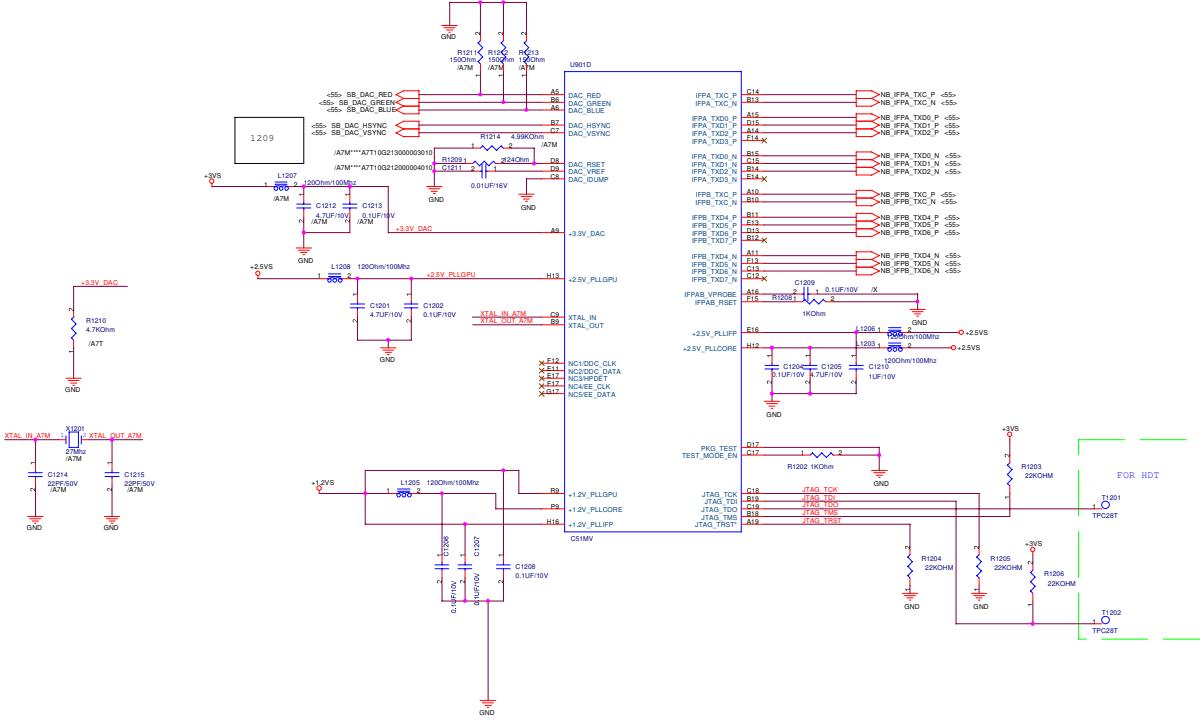
<< Kennedy\_Zhang >>

<41> PE\_RXD[0..15] ——————> PE\_TXD[0..15] <41>  
 <41> PE\_RXM[0..15] ——————> PE\_TXM[0..15] <41>



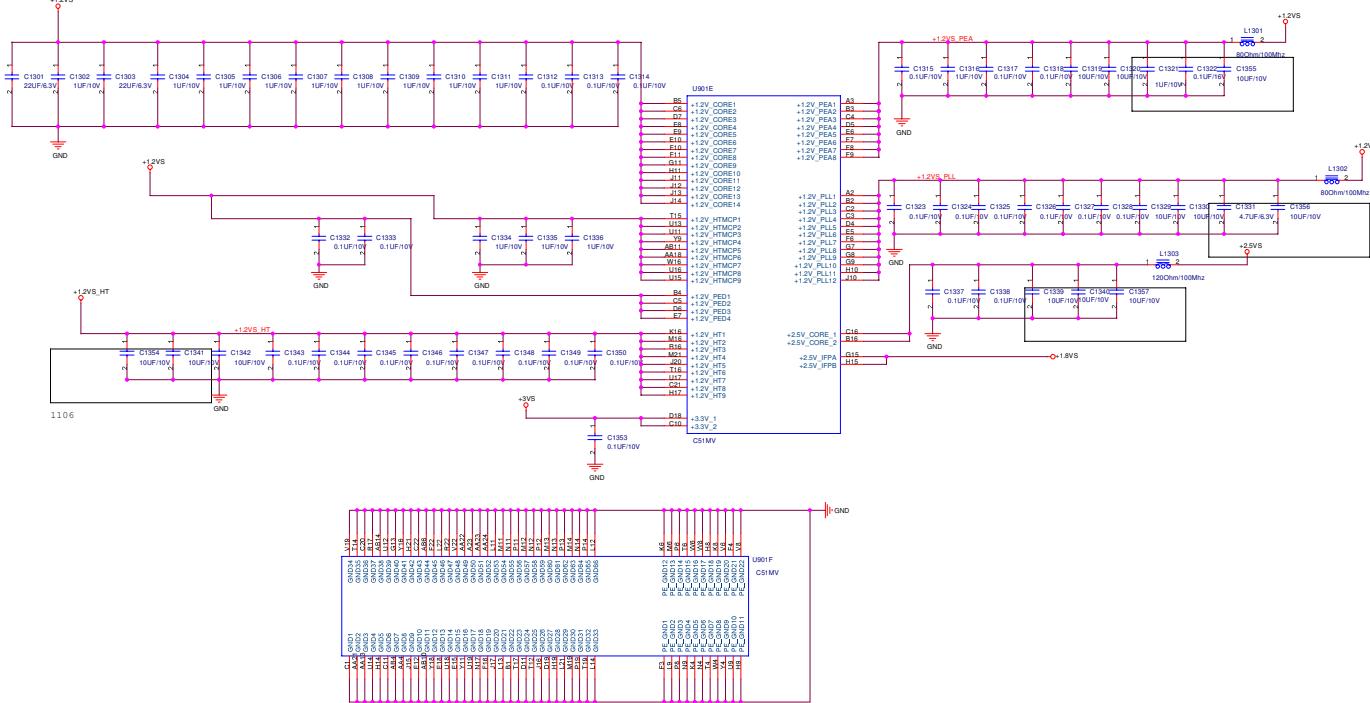
**ASUS** Title : C51M PCIEx16  
 ASUSTECH Project Name : **ATT** Engineer: **PENG XIAO**  
 Date: 2008-11-02, 2008 Sheet 11 of 79 Rev 2.0

<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>

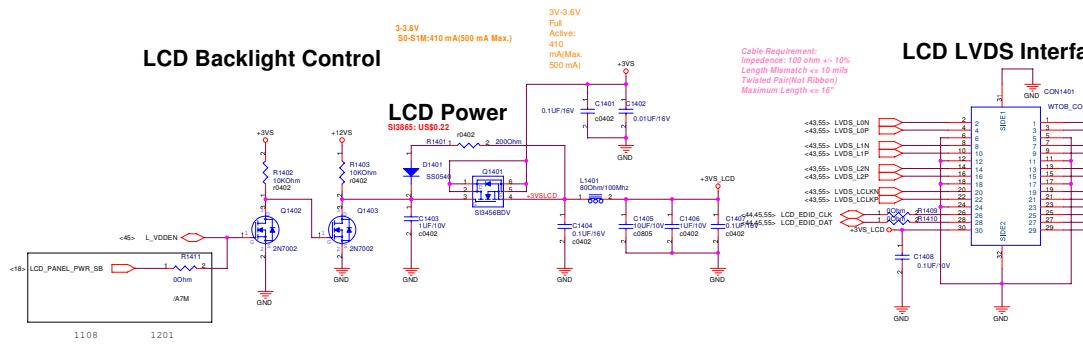




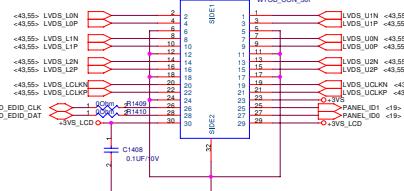
<< Kennedy\_Zhang >>



## LCD Backlight Control

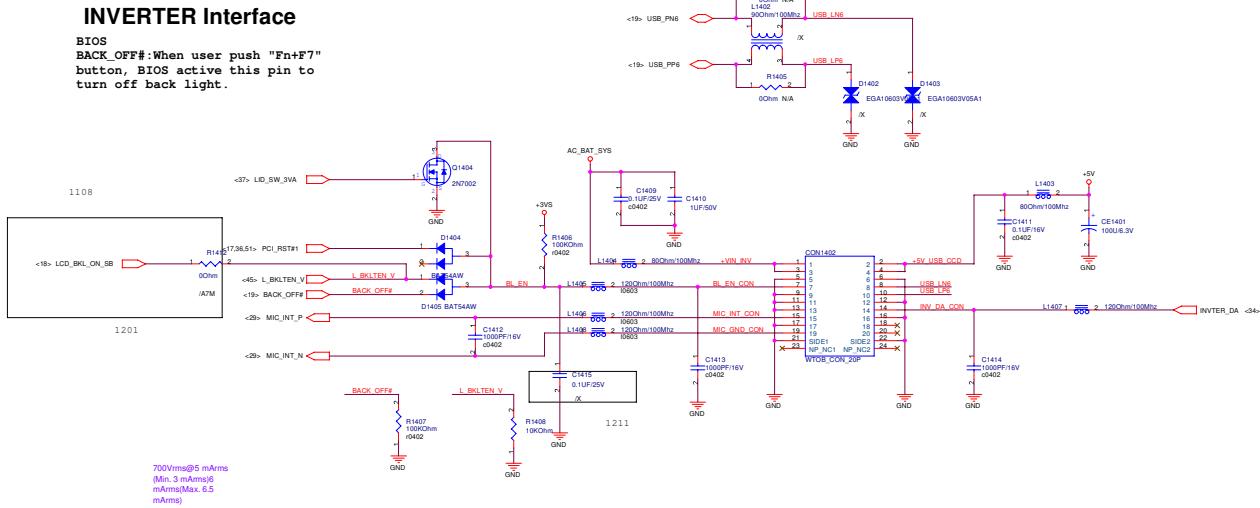


## LCD LVDS Interface



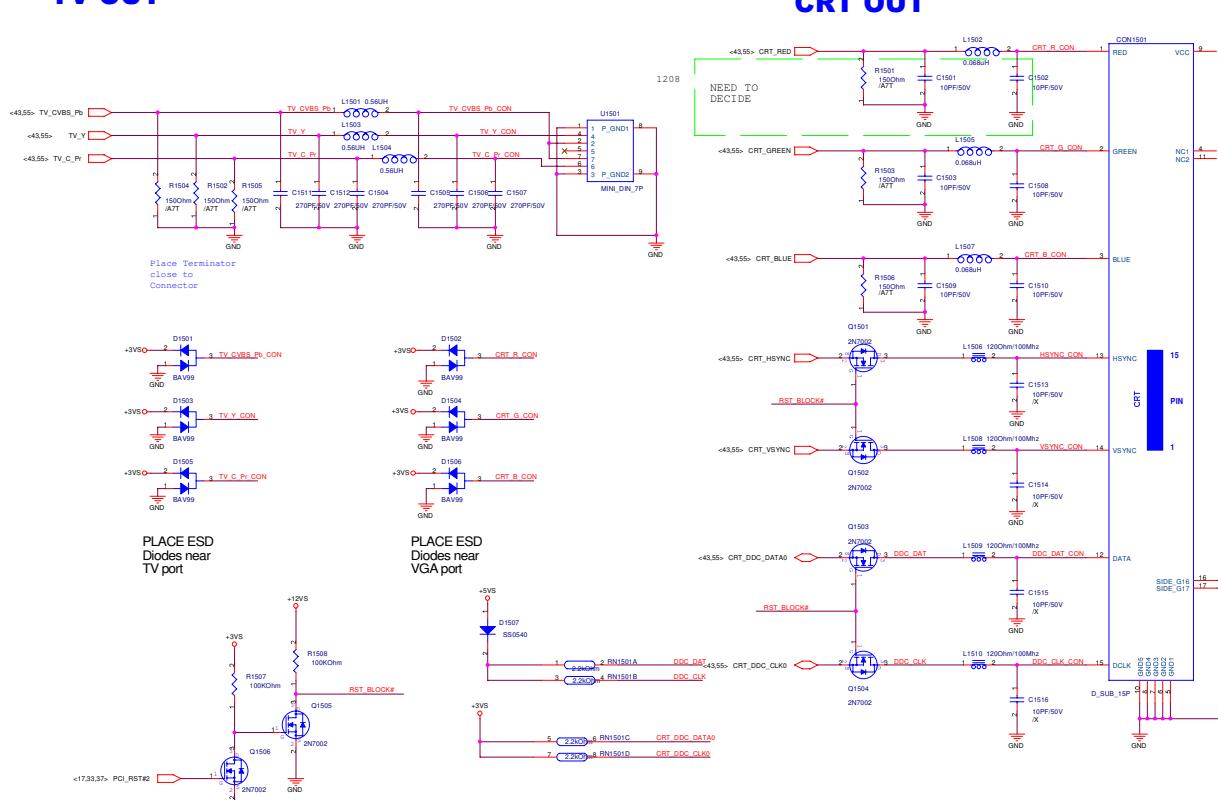
## INVERTER Interface

**BIOS**  
BACK\_OFF#: When user push "Fn+F7" button, BIOS active this pin to turn off back light.



<< Kennedy\_Zhang >>

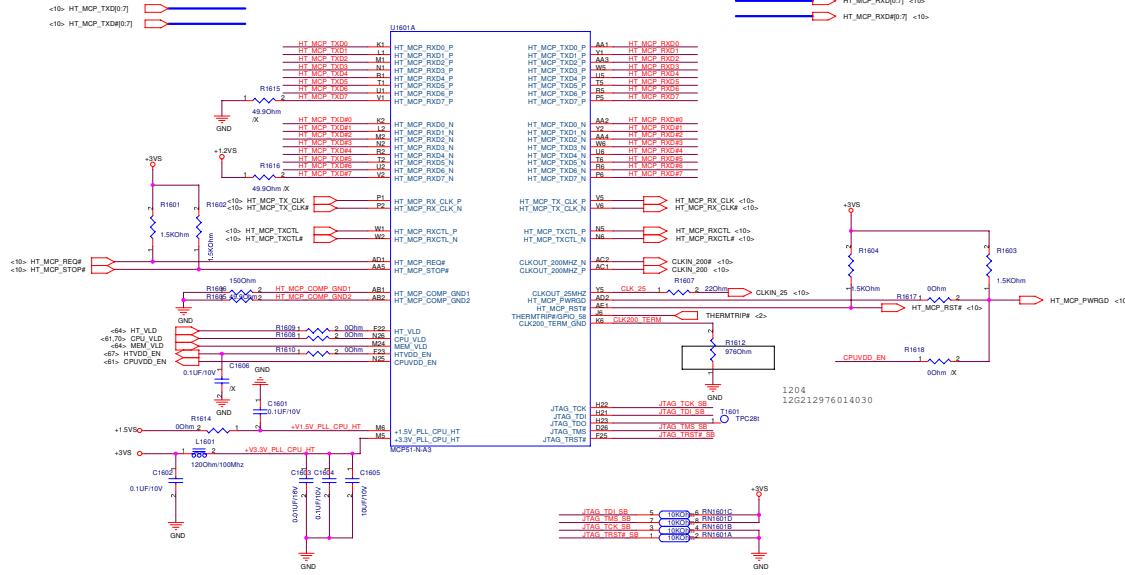
**TV OUT**



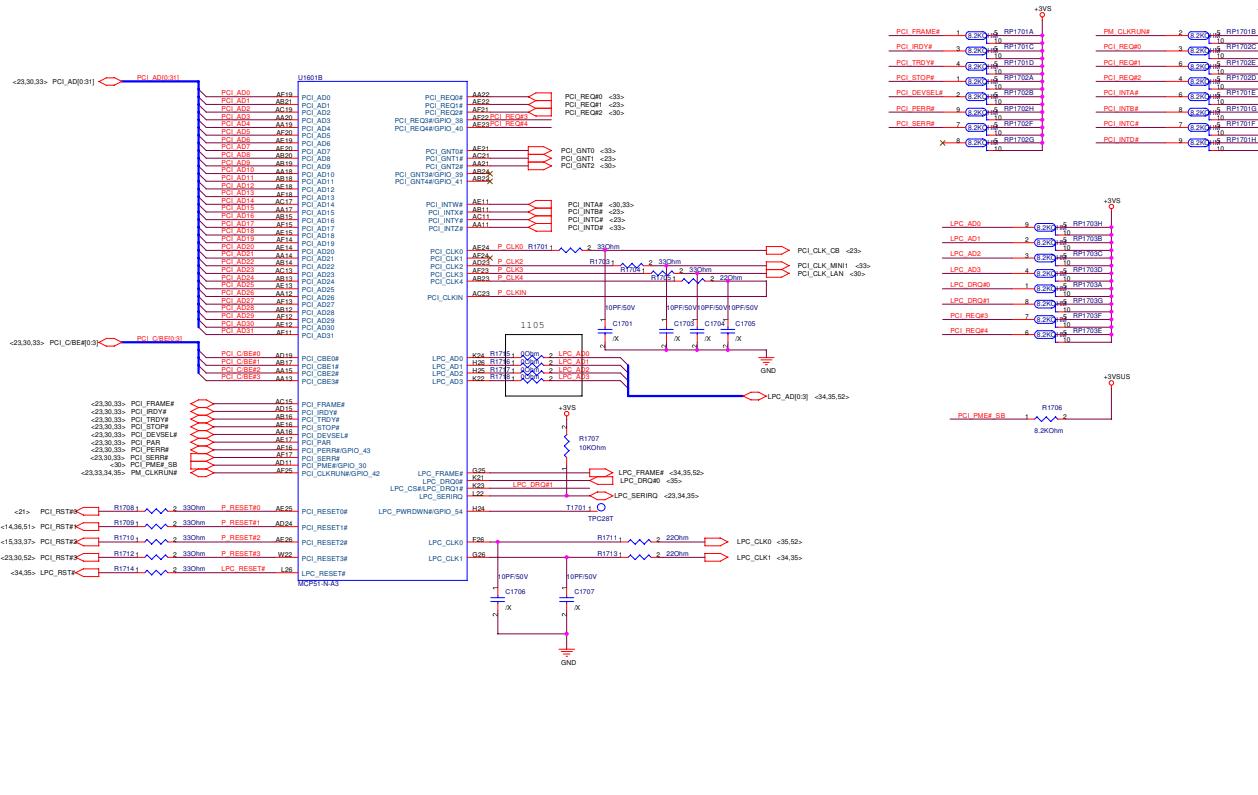
<< Kennedy\_Zhang >>

**ASUS** Title : **CRT TV CONNECTER**  
 ASUSTECH Engineer: **PENG\_XIAO**

Size	Project Name	Rev
<b>C</b>	<b>AT&amp;T</b>	<b>2.0</b>

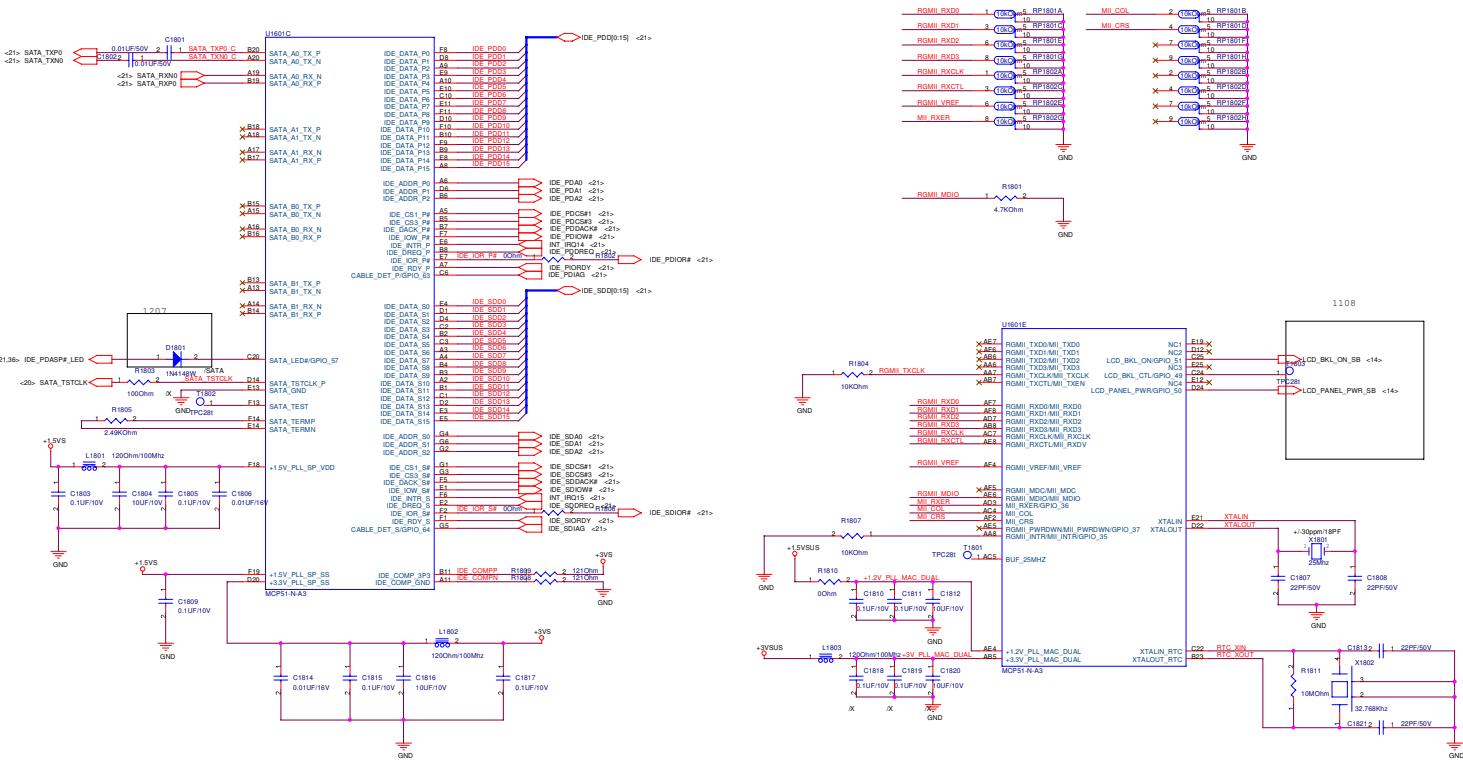


<< Kennedy\_Zhang >>

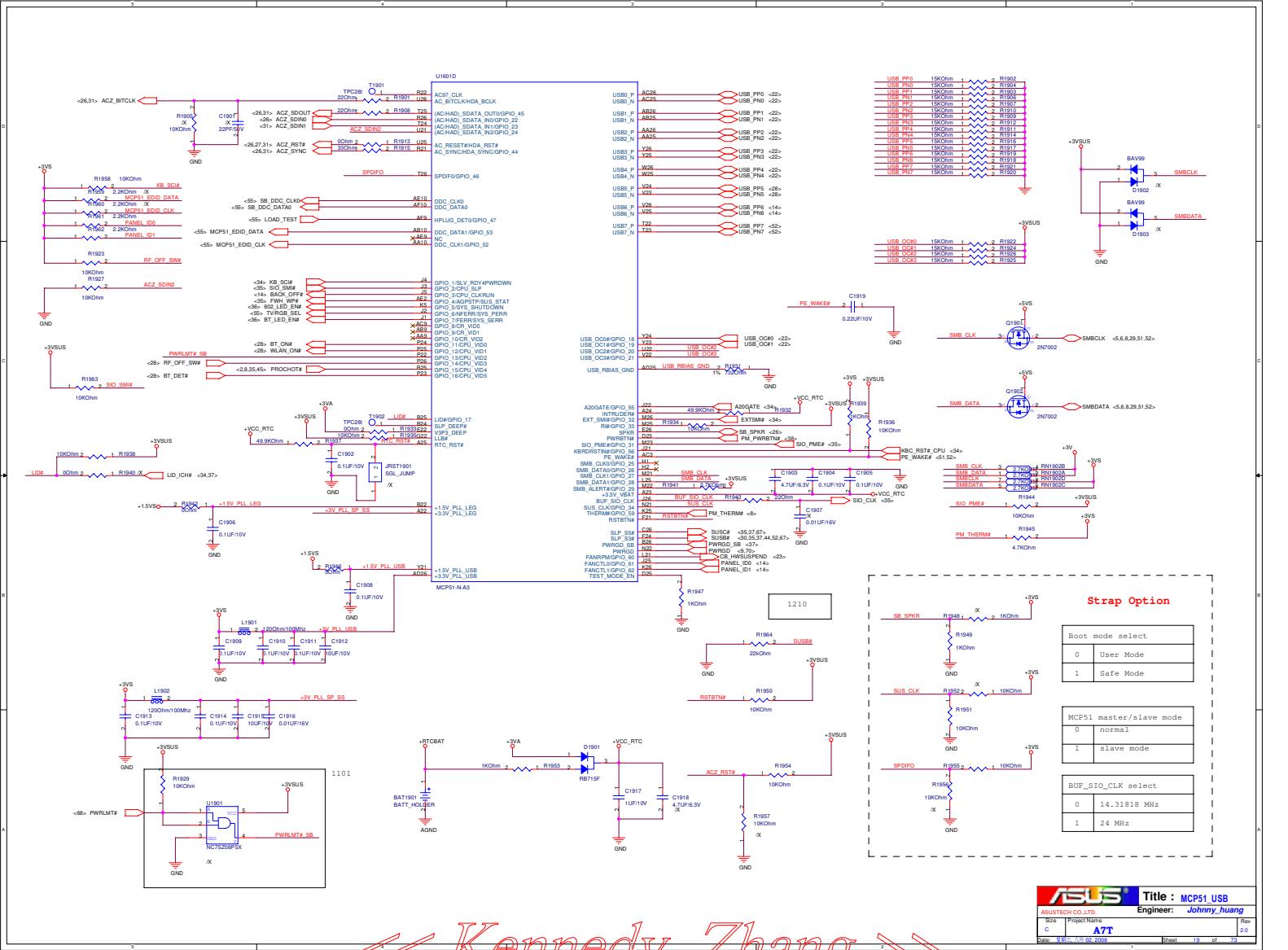


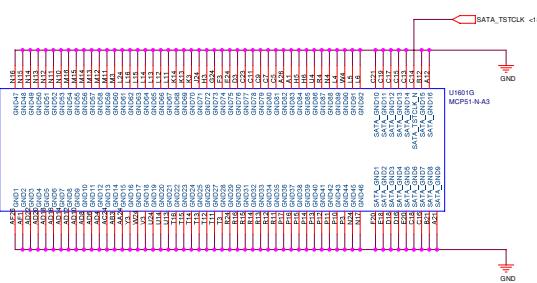
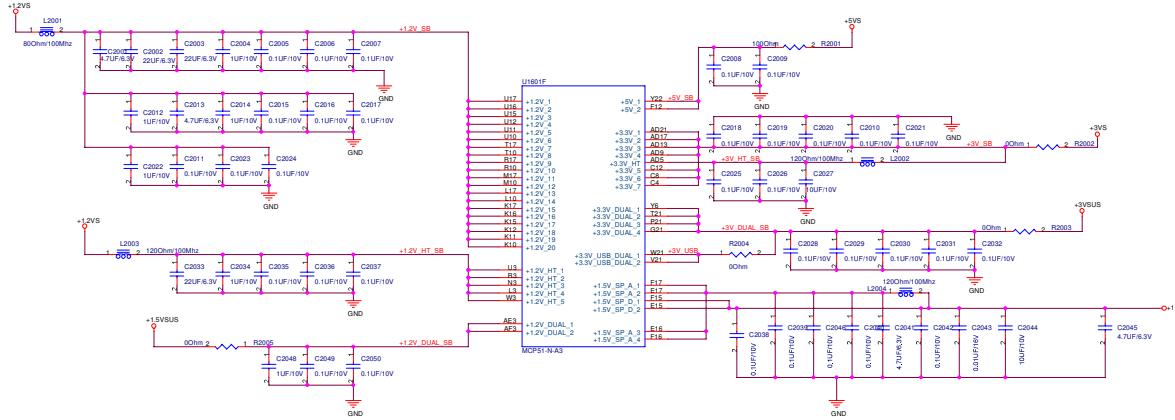
<< Kennedy\_Zhang >>





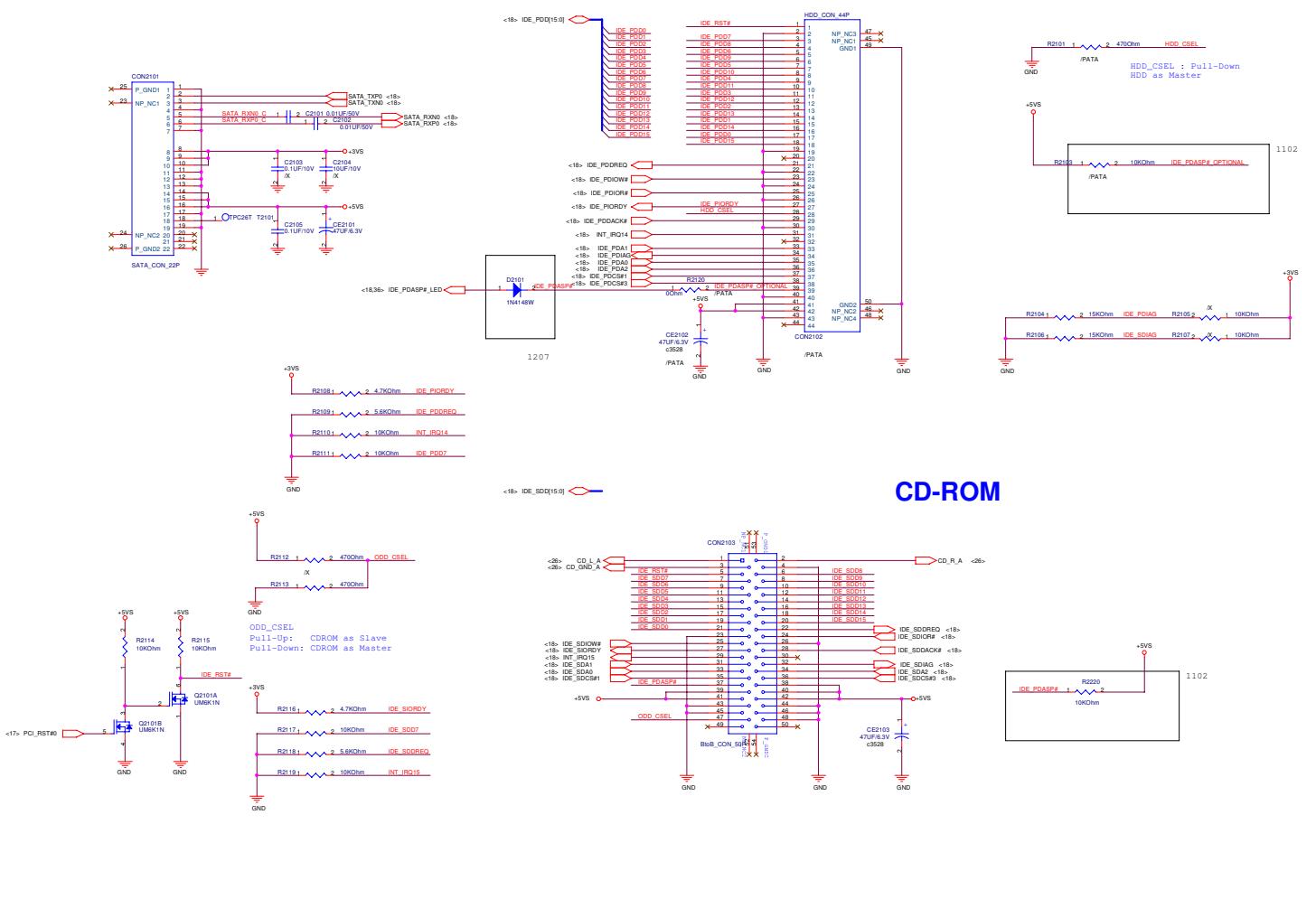
<< Kennedy\_Zhang >>



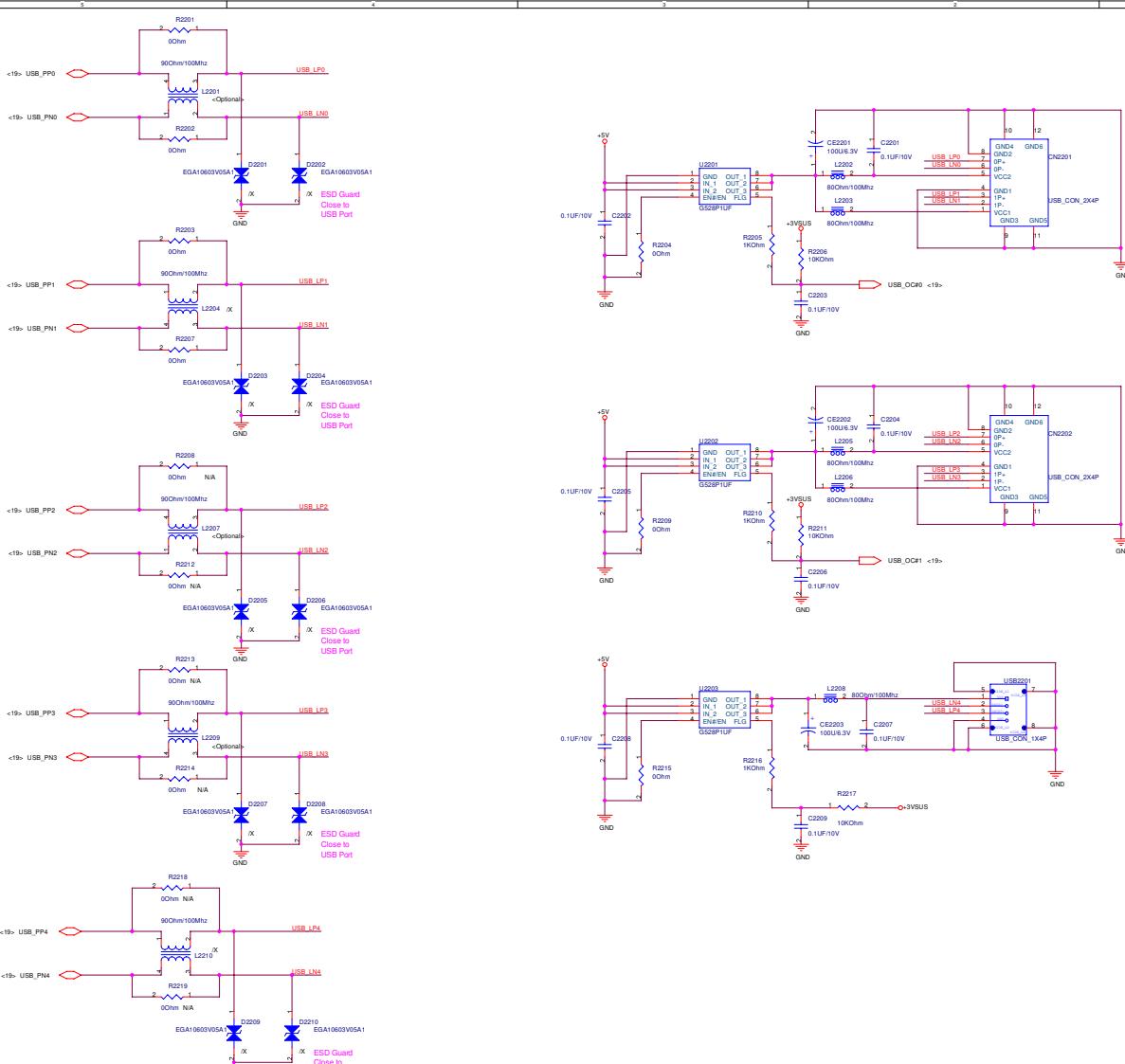


**ASUS** Title : MCP51 PWR  
 ASUSTECH CO., LTD. Engineer: Johnny\_huang  
 S024 Project Name: ATT Rev 2.0  
 Date: 08/01/2008 Sheet 20 of 79

<< Kennedy\_Zhang >>

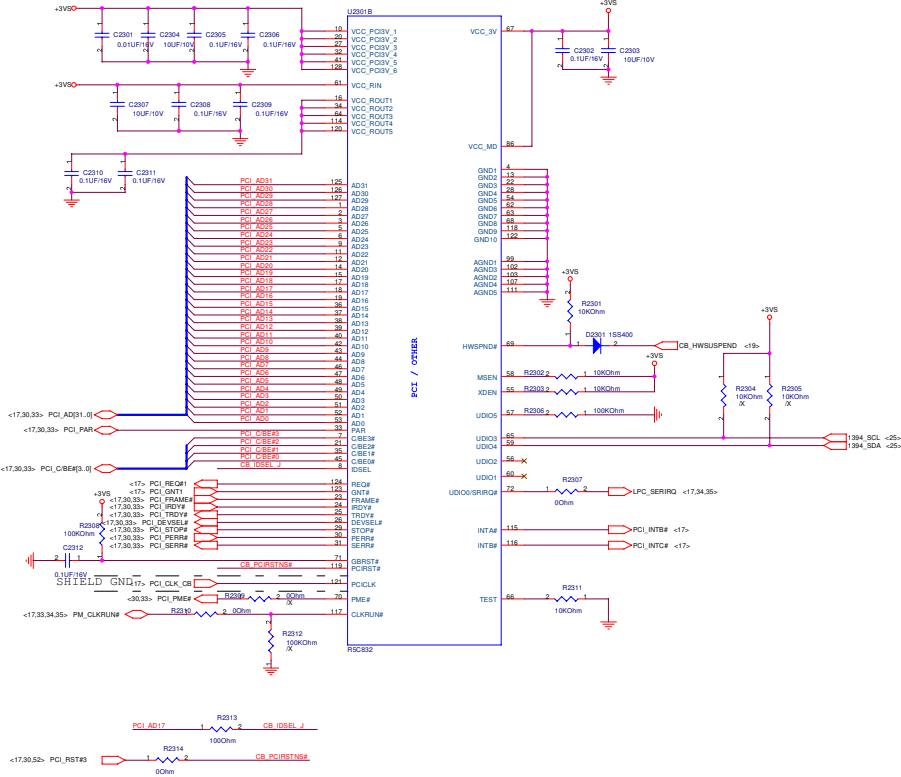


<< Kennedy\_Zhang >>

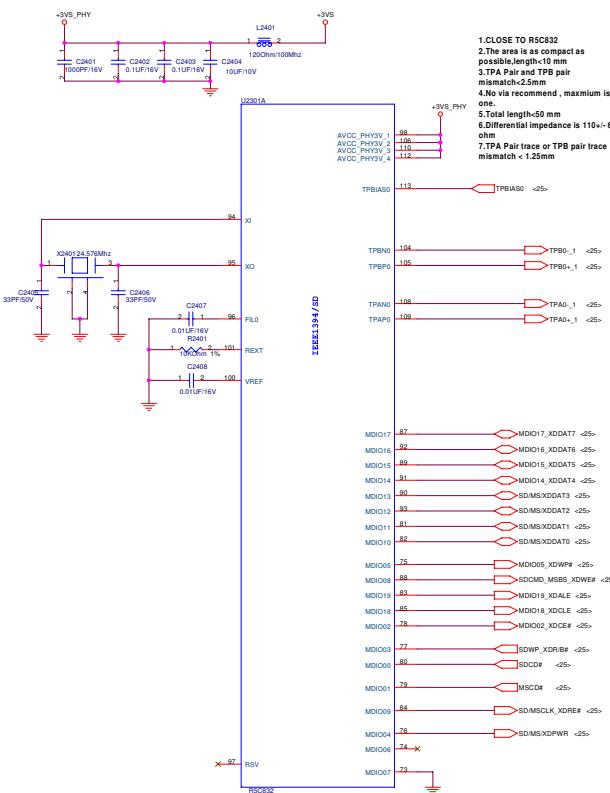


<< Kennedy\_Zhang >>

<b>ASUS</b>	Title : USB
ASUSTECH CO., LTD.	Engineer: Johnny_huang
C ATT	Date: 08/07/04 2008
	Sheet 22 of 79

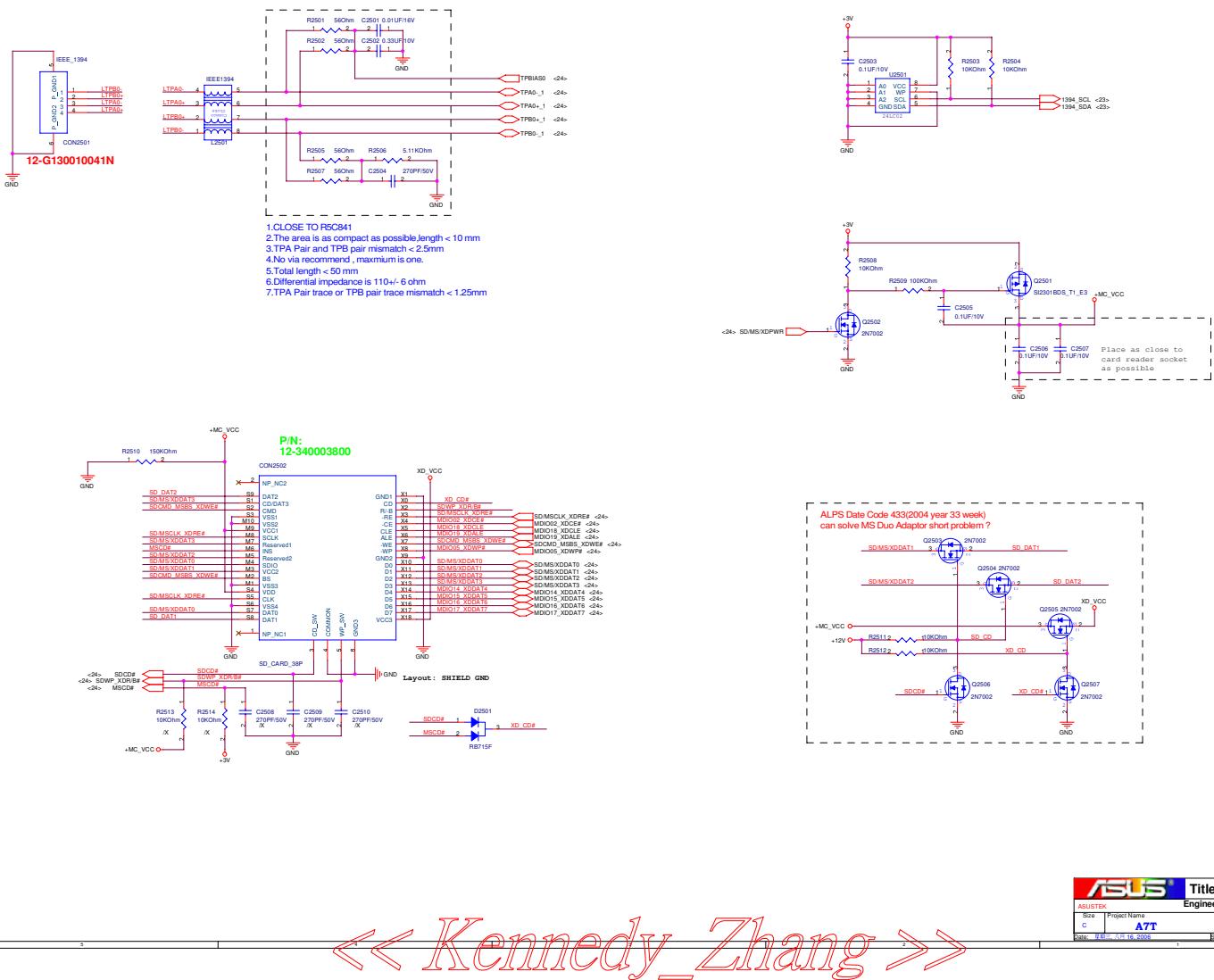


<< Kennedy\_Zhang >>

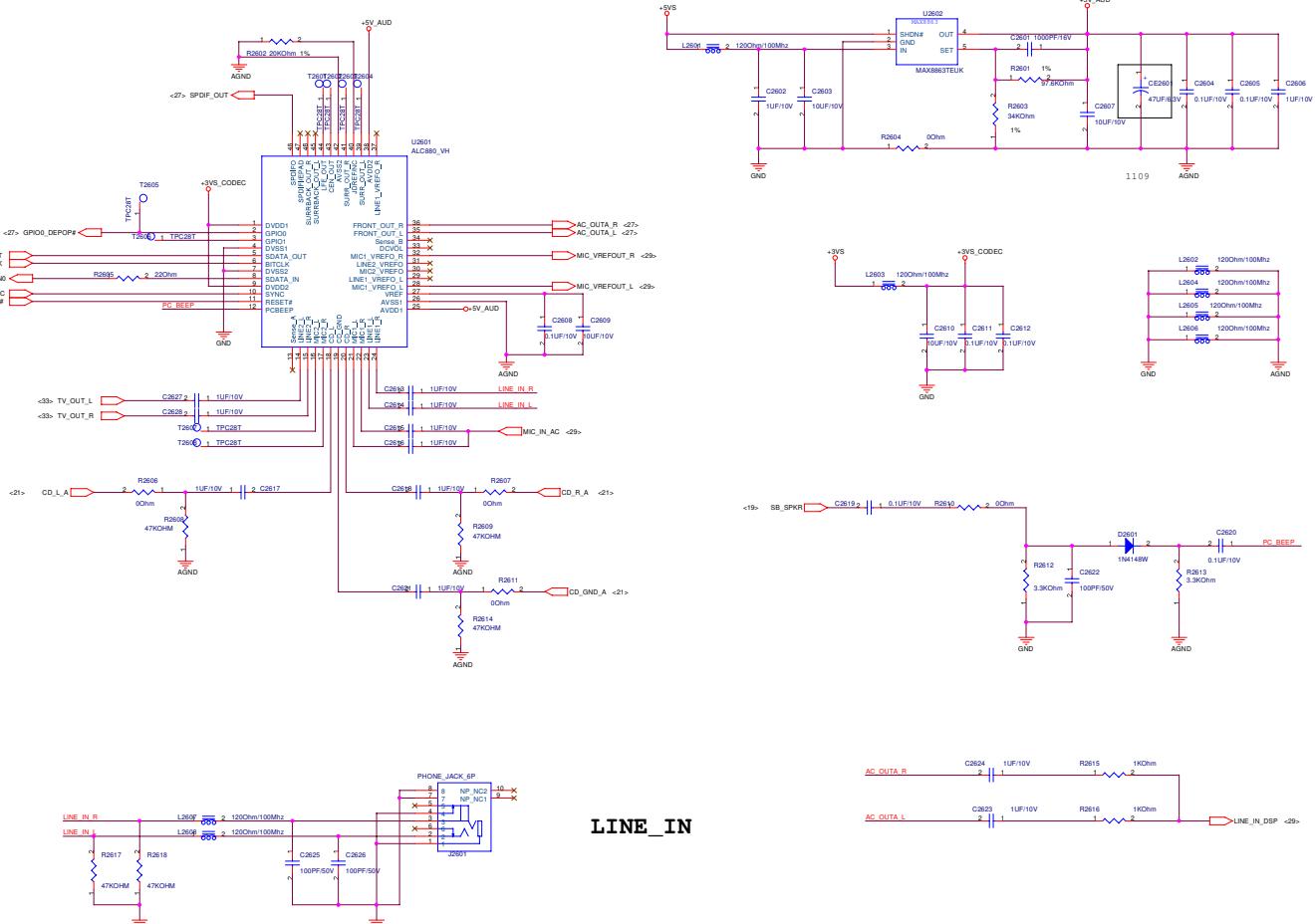


**ASUS** Title : RSC832\_2  
 ASUSTEK Project Name : **ATT** Engineer: **echo\_xing**  
 Date: 2008-11-02 2008 Sheet 24 of 79 Rev 2.0

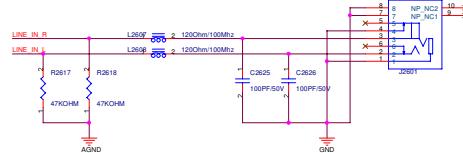
<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>

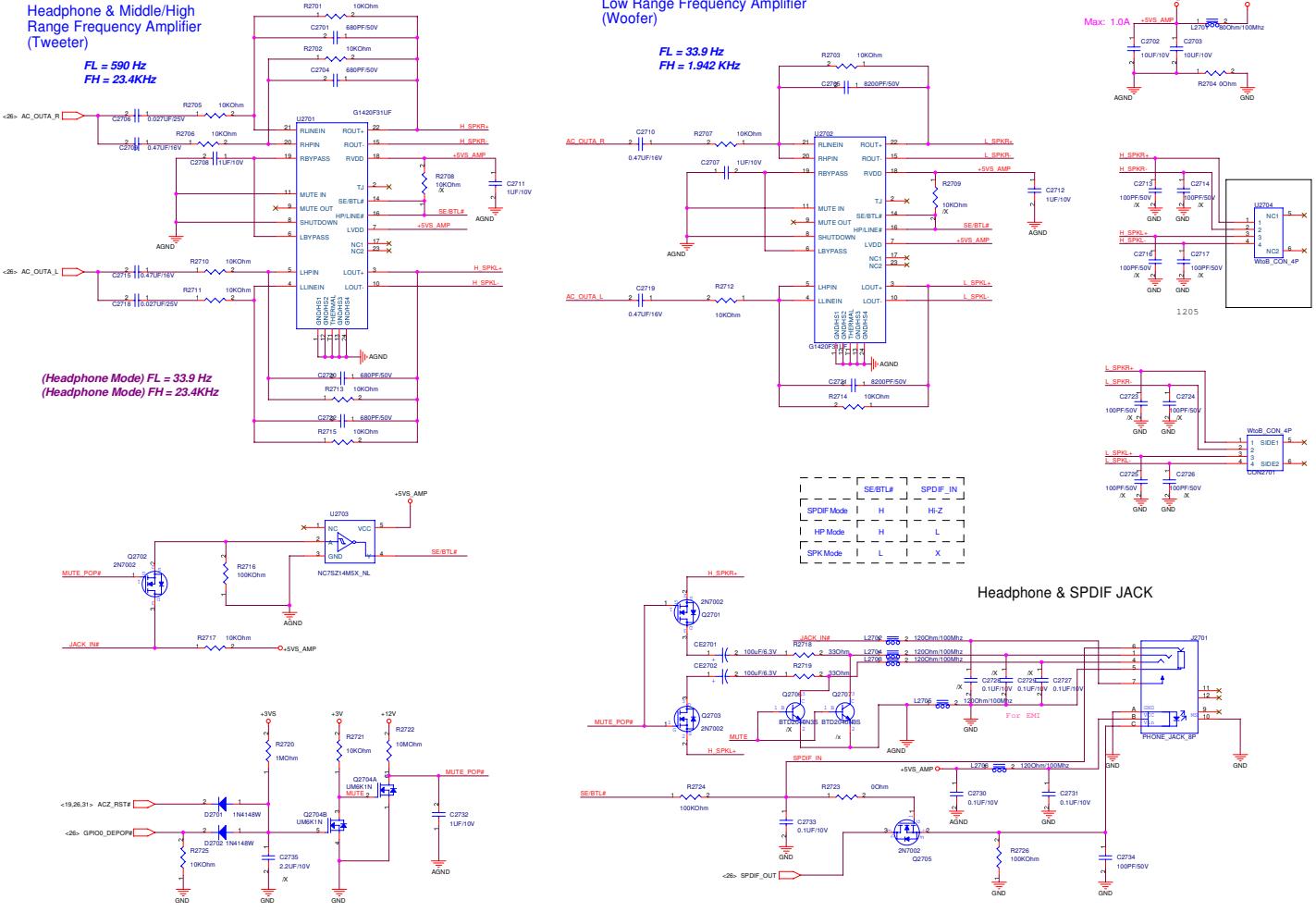


### LINE\_IN



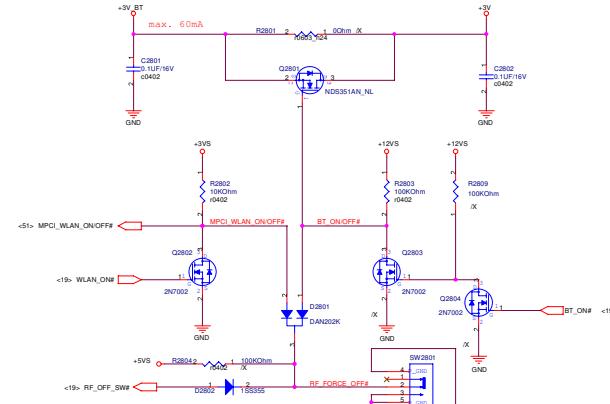
<< Kennedy\_Zhang >>

<b>ASUS</b>	Title : ALC880
ASUSTEK	Engineer: echo_xing
S024	Project Name: ATT
Date: 08/22/2008	Sheet 26 of 79

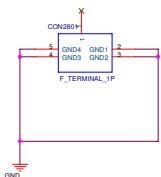


<< Kennedy\_Zhang >>

### WLAN/BT ON/OFF Control

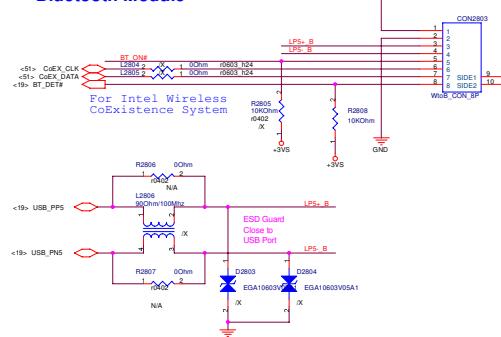


### ATV\_DTV\_FM Antenna

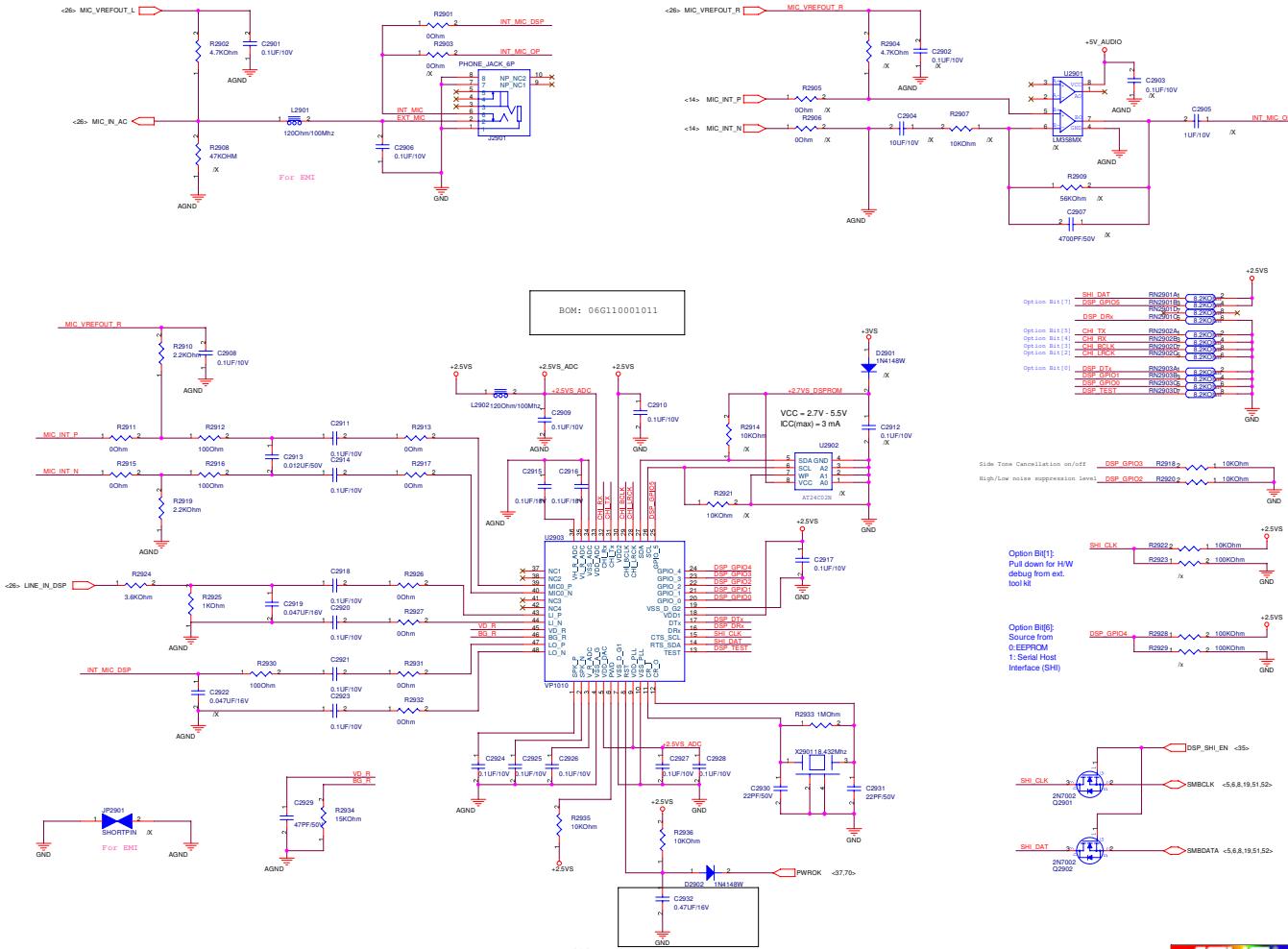


14G152075000

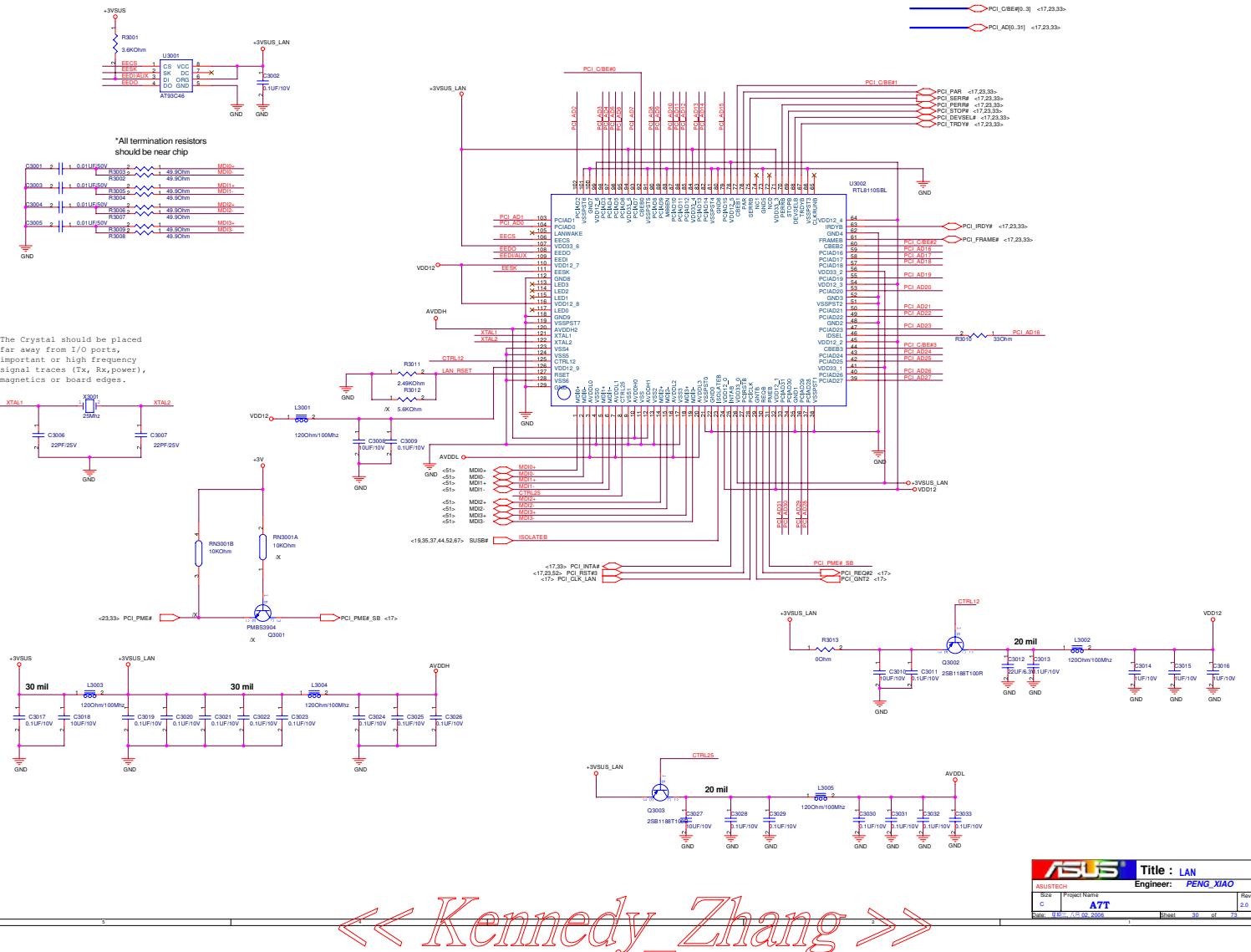
### Bluetooth Module



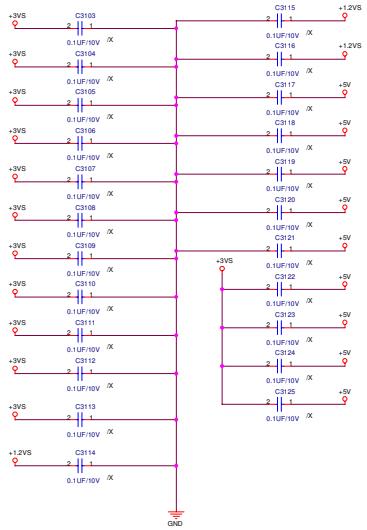
<< Kennedy\_Zhang >>



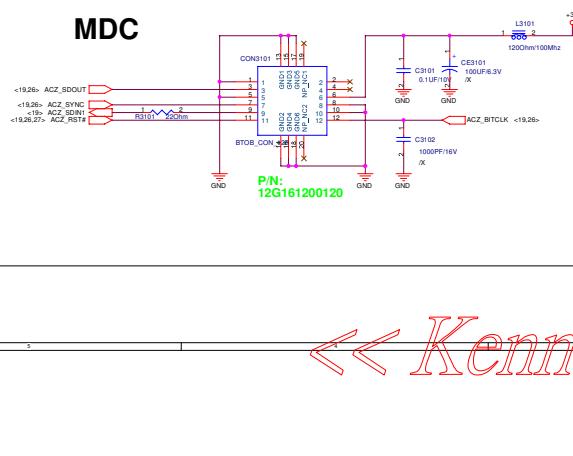
<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>

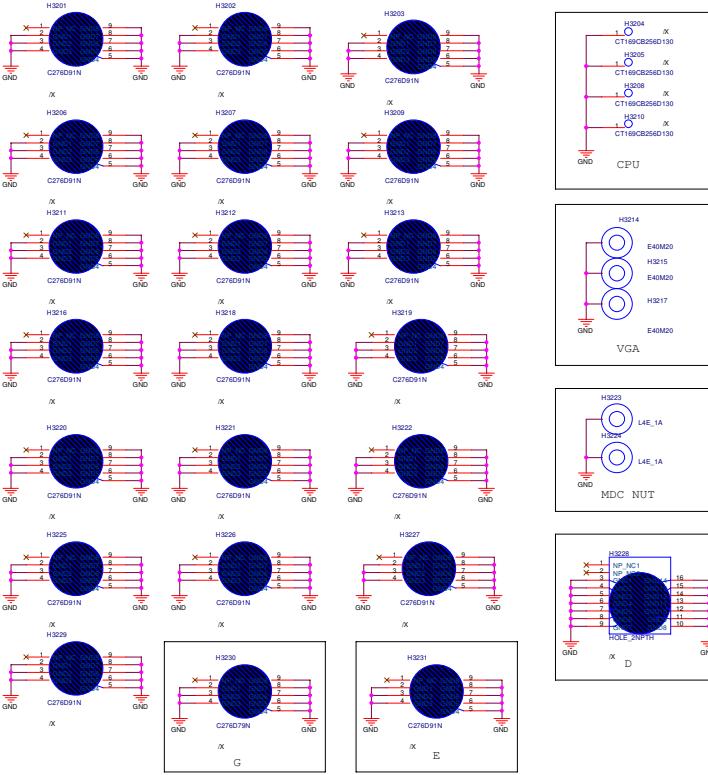


### MDC



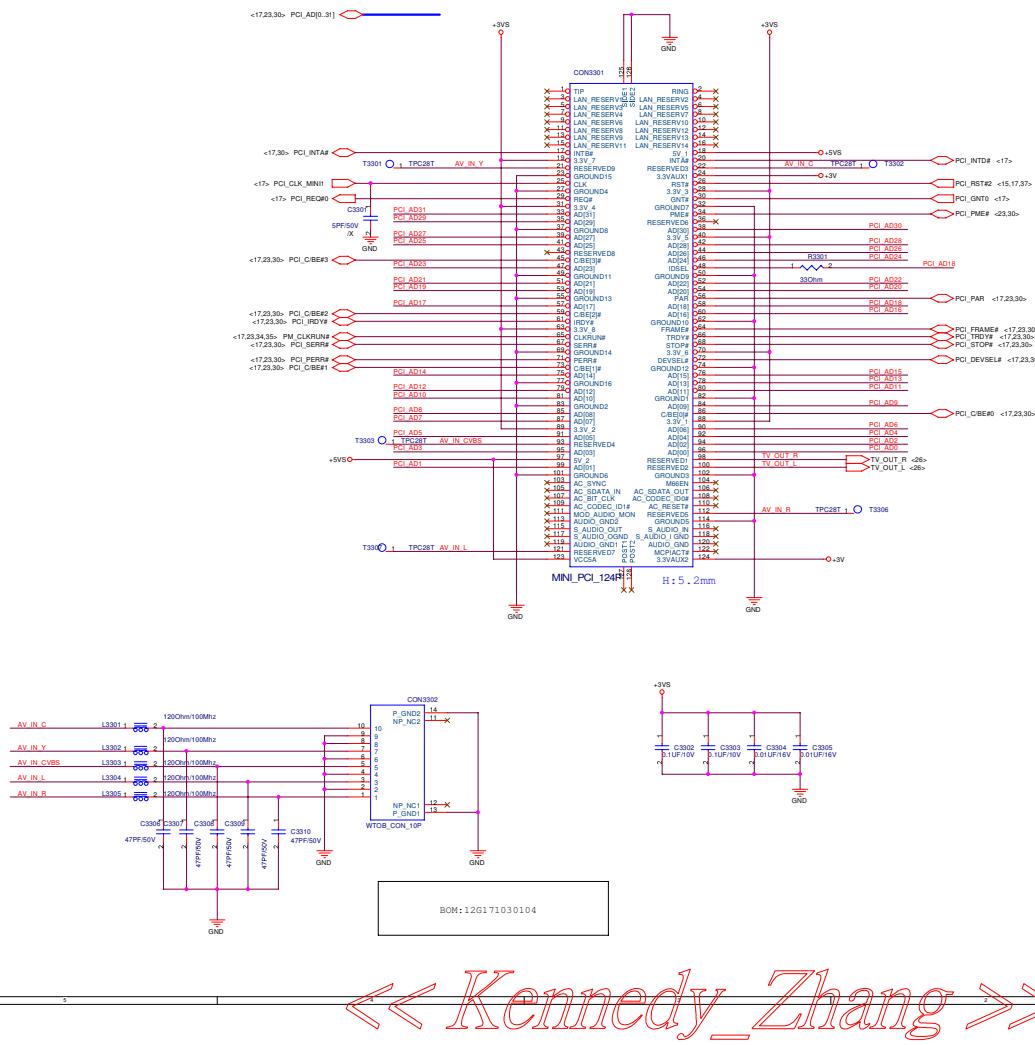
**ASUS** Title : MDC  
 ASUSTECH Project Name : ATT Rev 2.0  
 Date: 08/01/2008 Engineer: PENG XIAO  
 Sheet 31 of 79

<< Kennedy\_Zhang >>

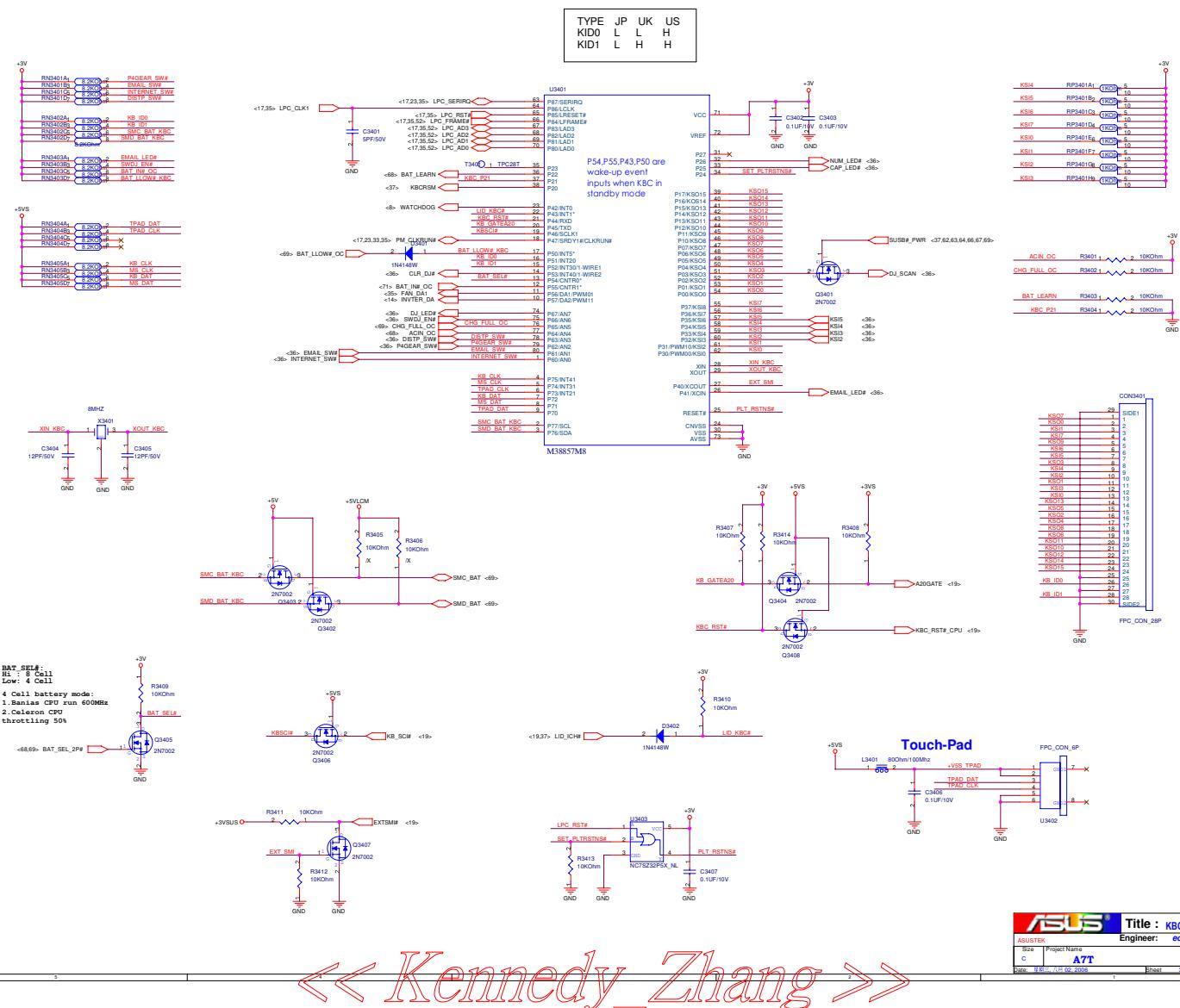


**ASUS** Title : Screw Hole  
 ASUSTEK Project Name : **ATT** Engineer: **echo\_xing**  
 Date: 08/01/2008 Rev: 2.0  
 Sheet 32 of 79

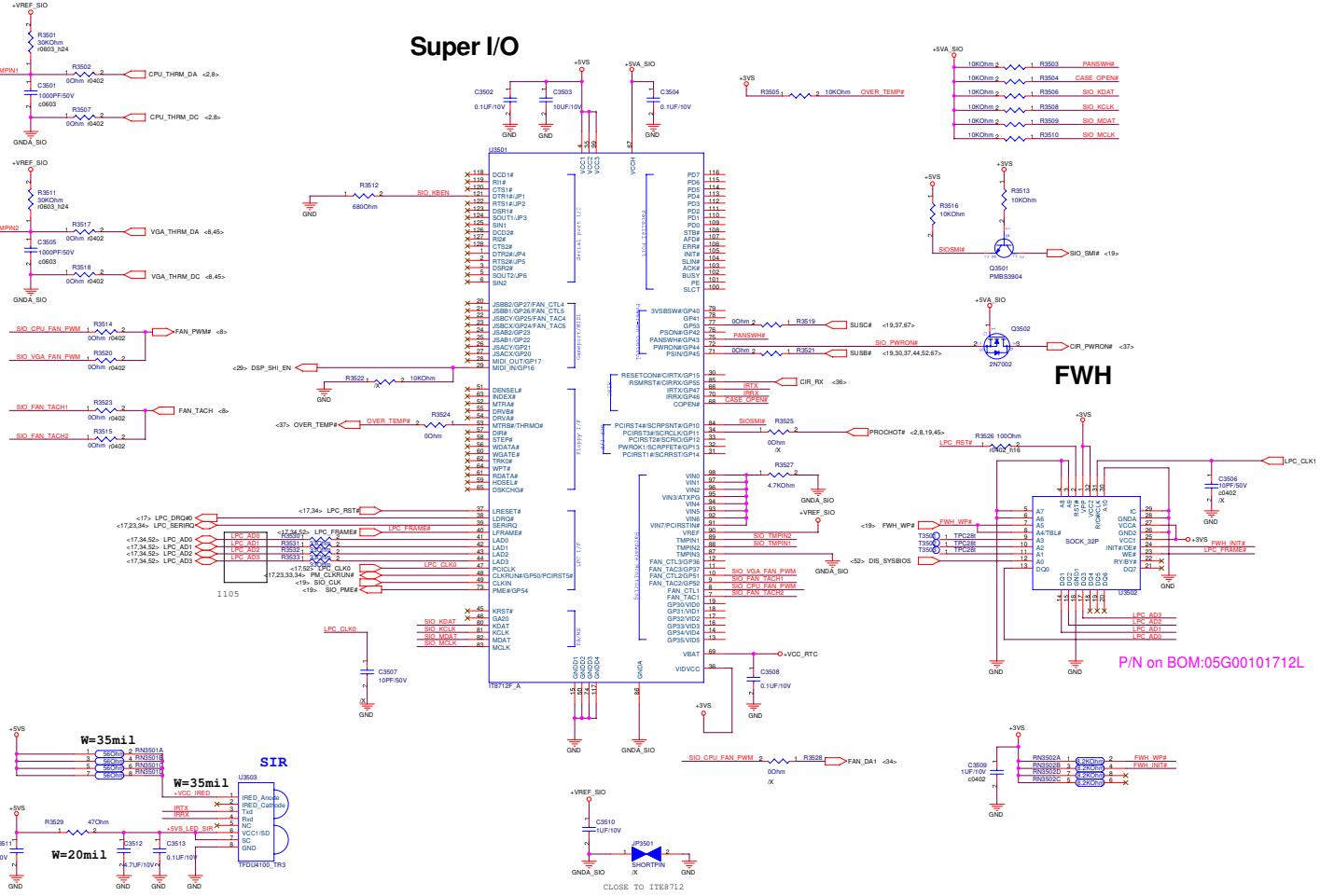
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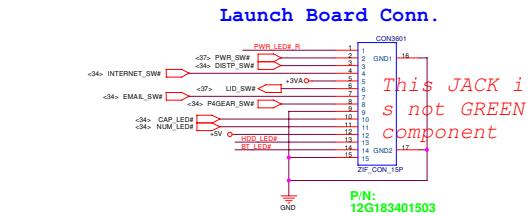


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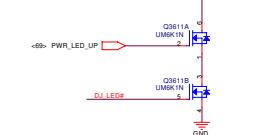
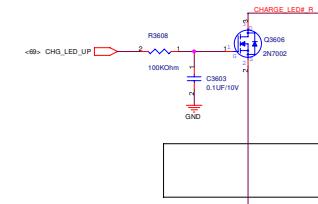
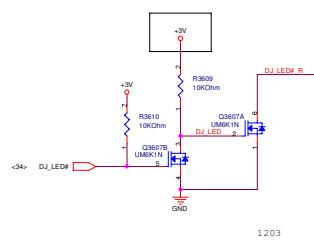
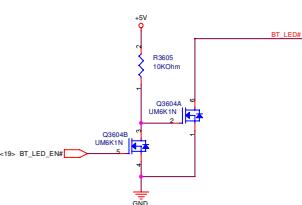
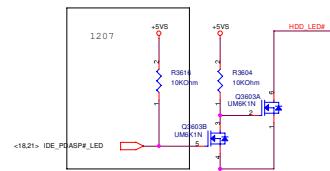
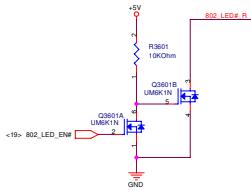
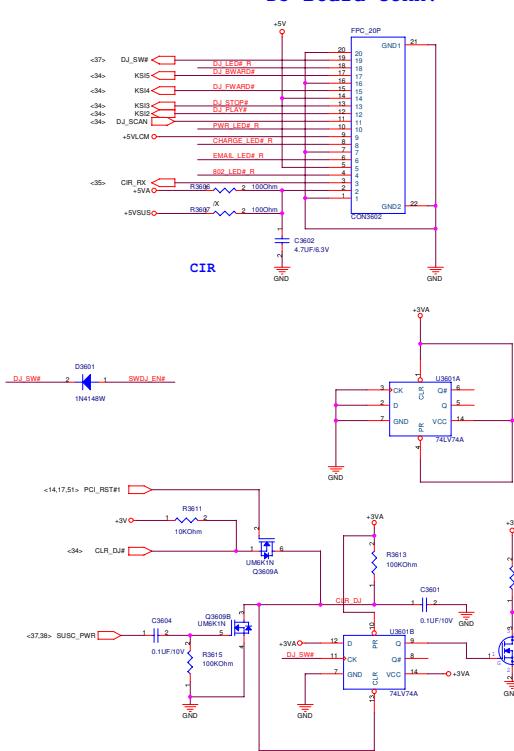


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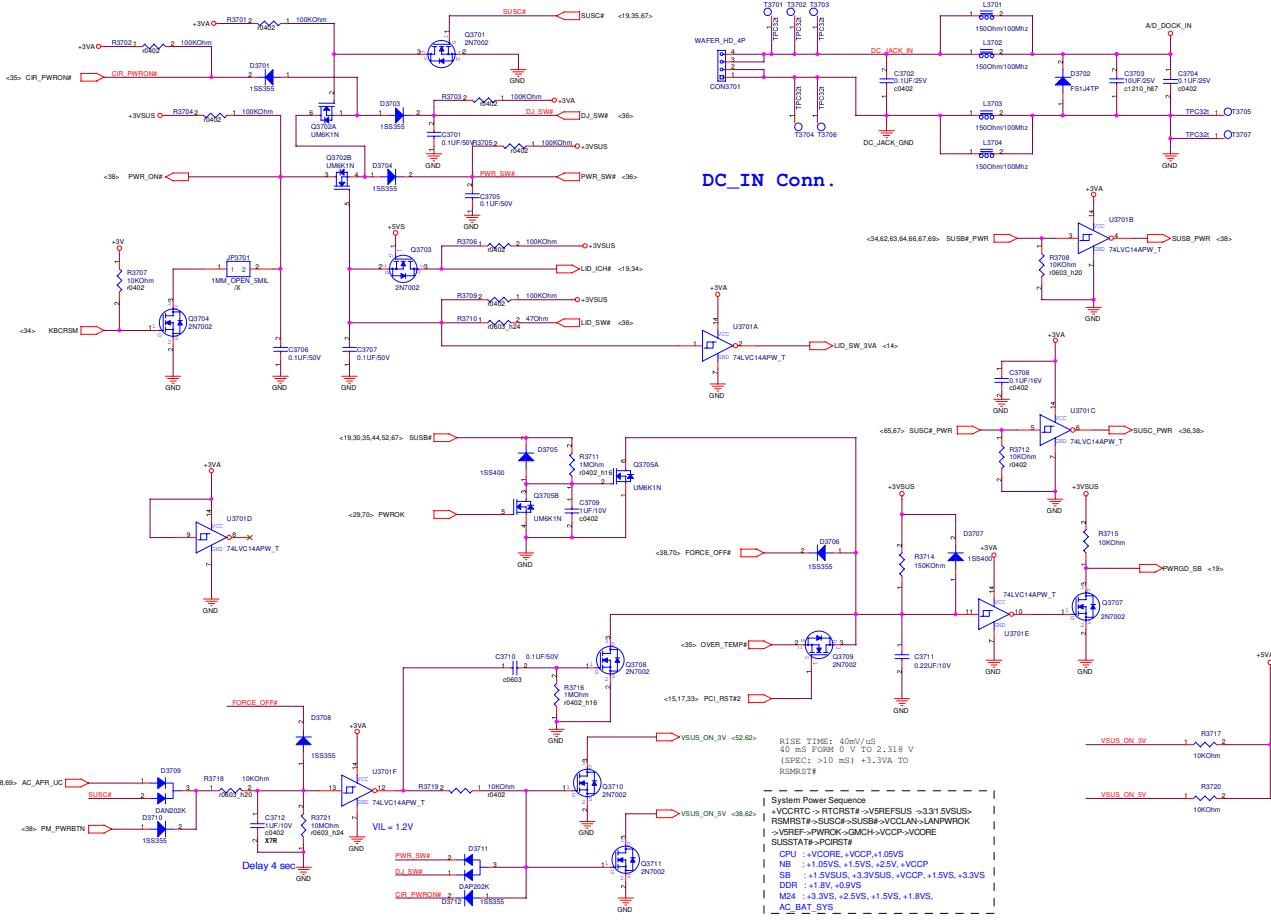
### Launch Board Conn.



### DJ Board Conn.

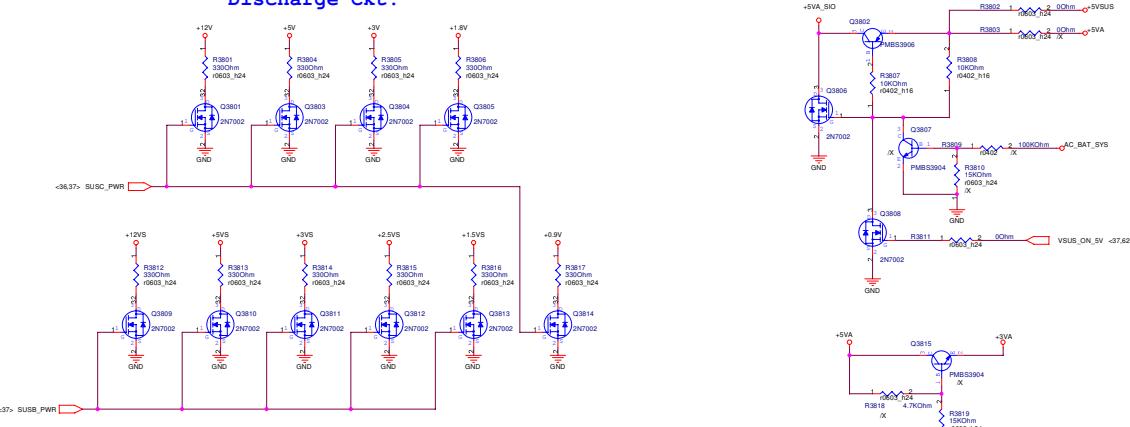


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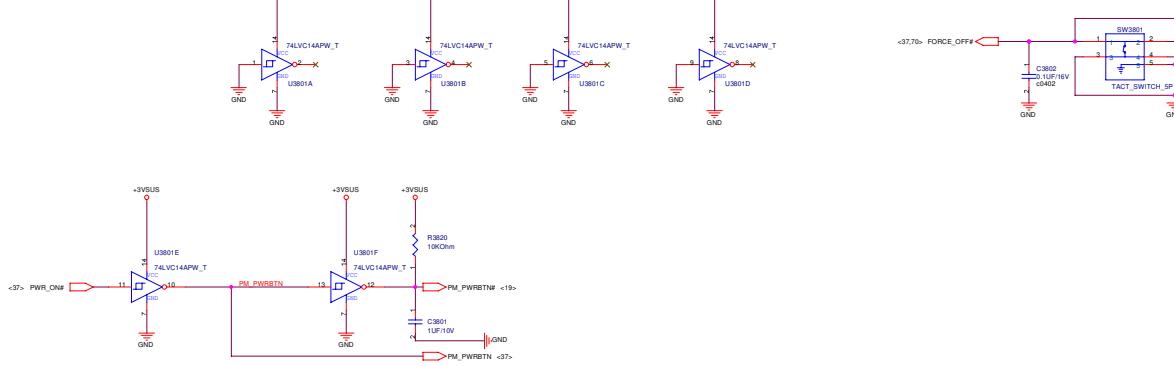


<< Kennedy\_Zhang >>

### Discharge Ckt.

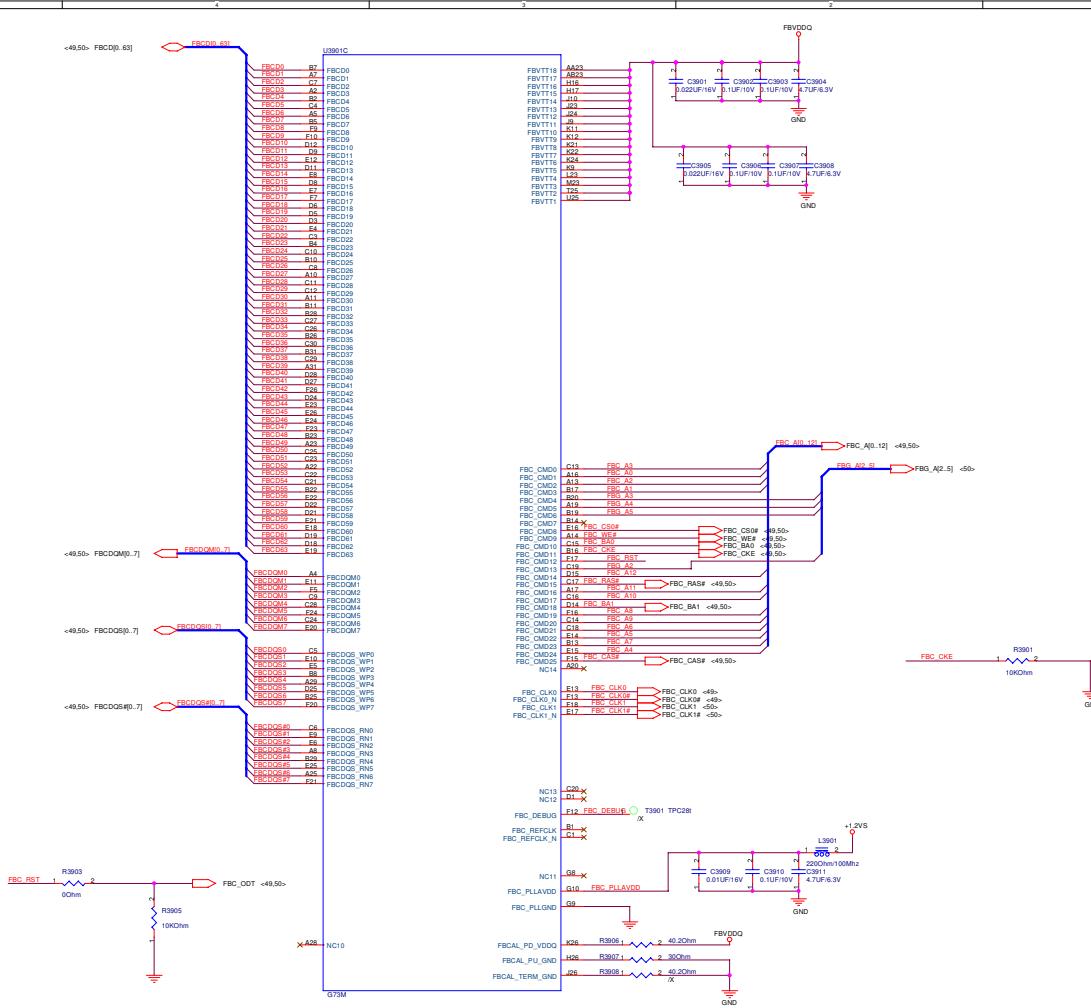


### RESET SW.

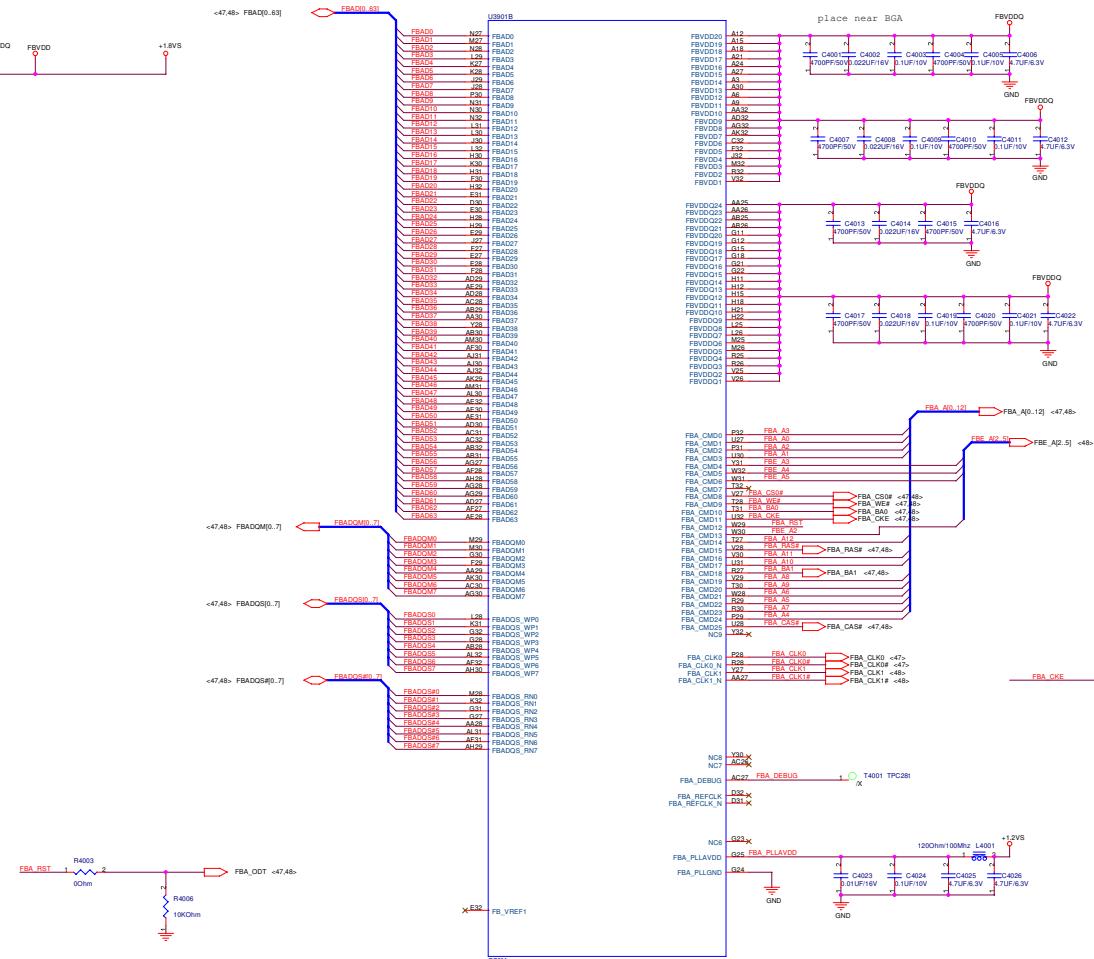


**ASUS** Title : PWR ON SEQ  
ASUSTECH Project Name : ATT Rev 2.0  
Date : 08/01/2008 Engineer : DEL\_TAN

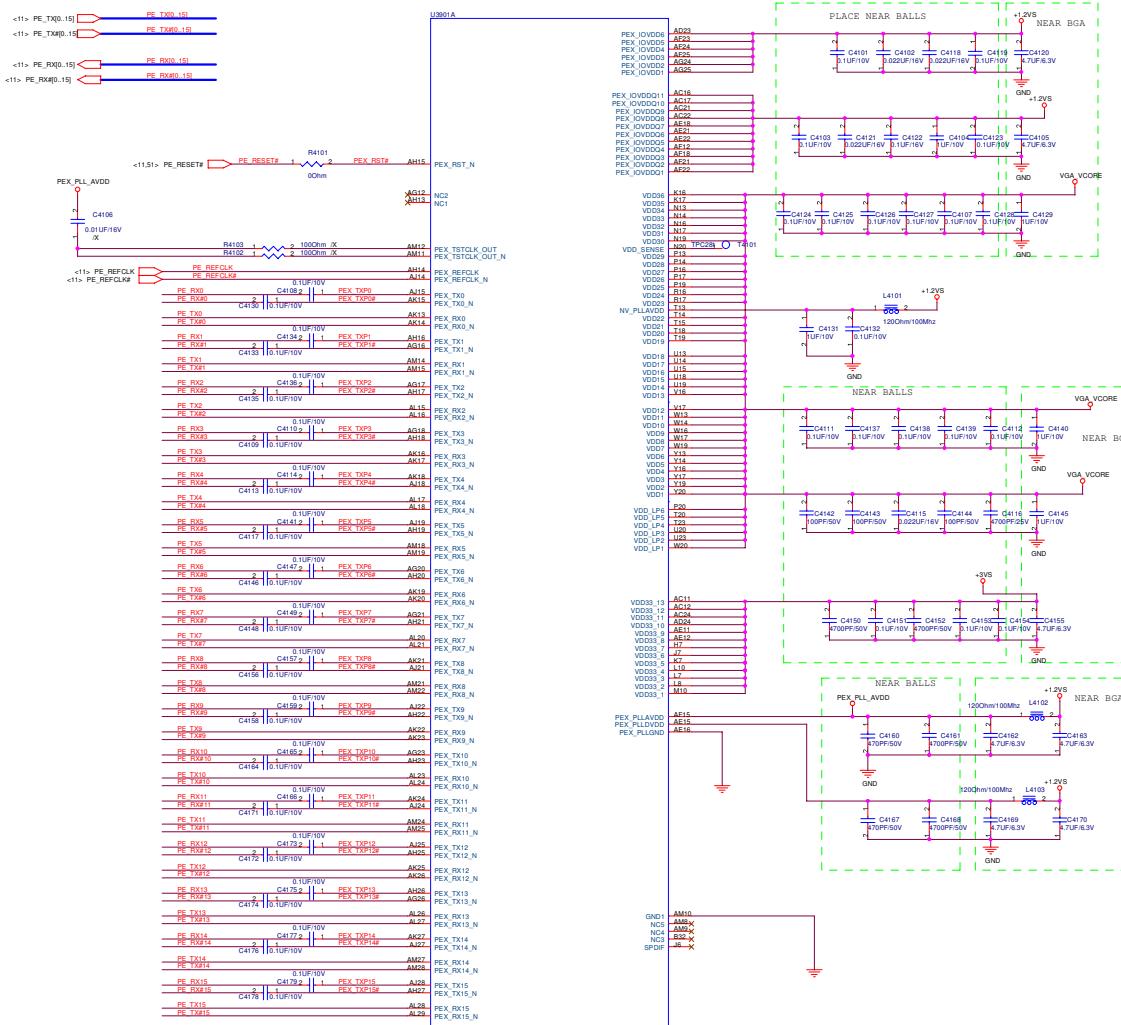
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<< Kennedy\_Zhang >>

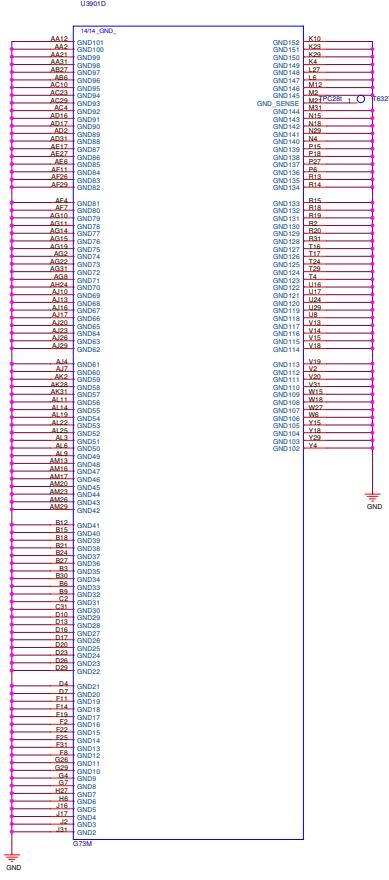


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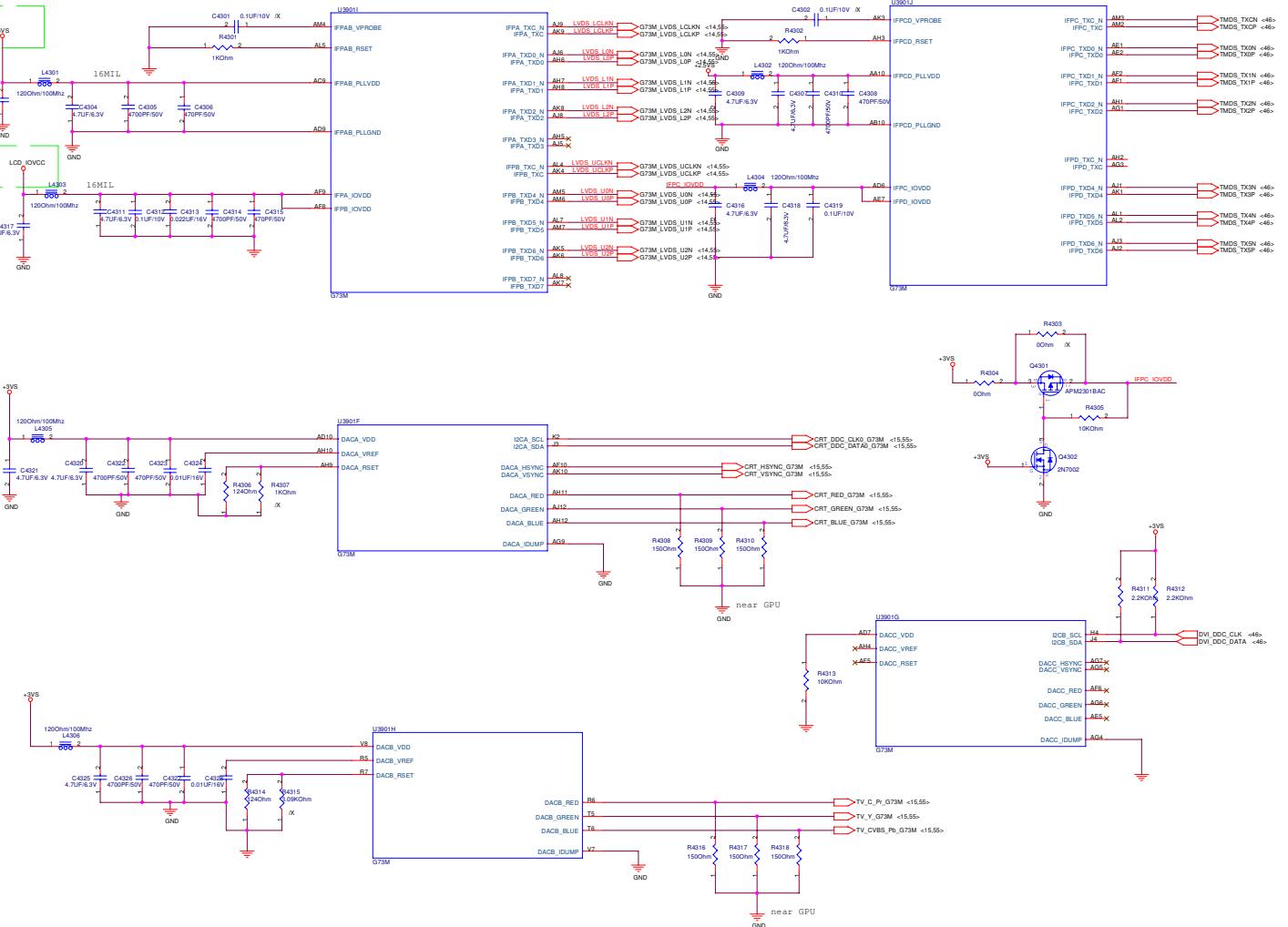
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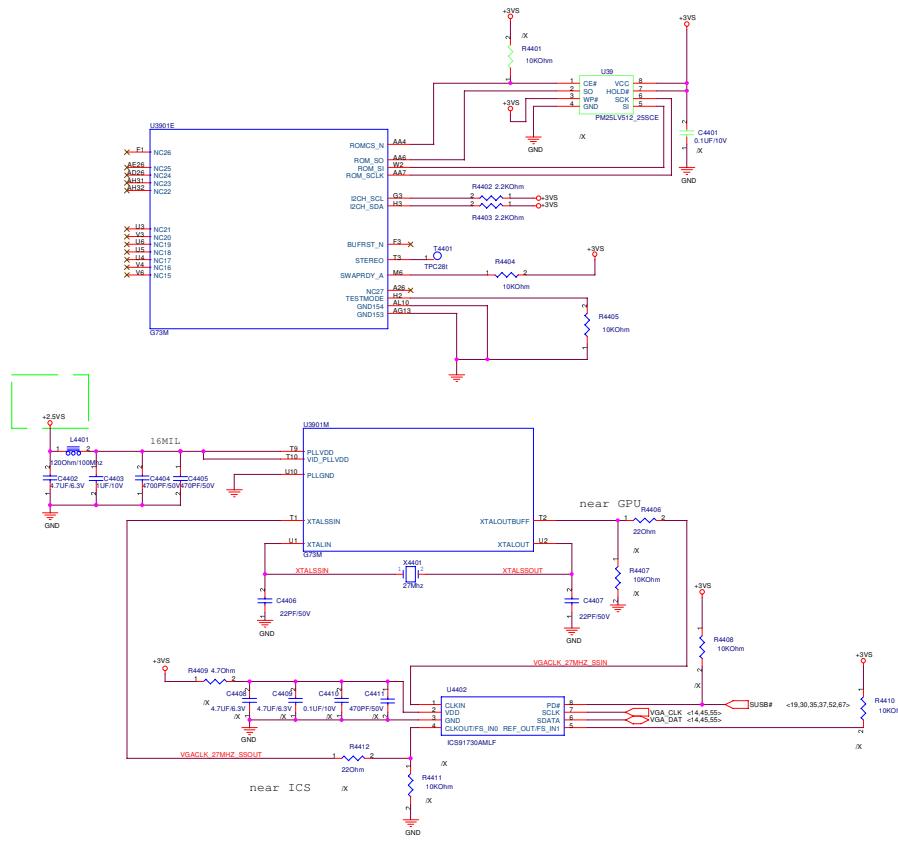
*<< Kennedy\_Zhang >>*



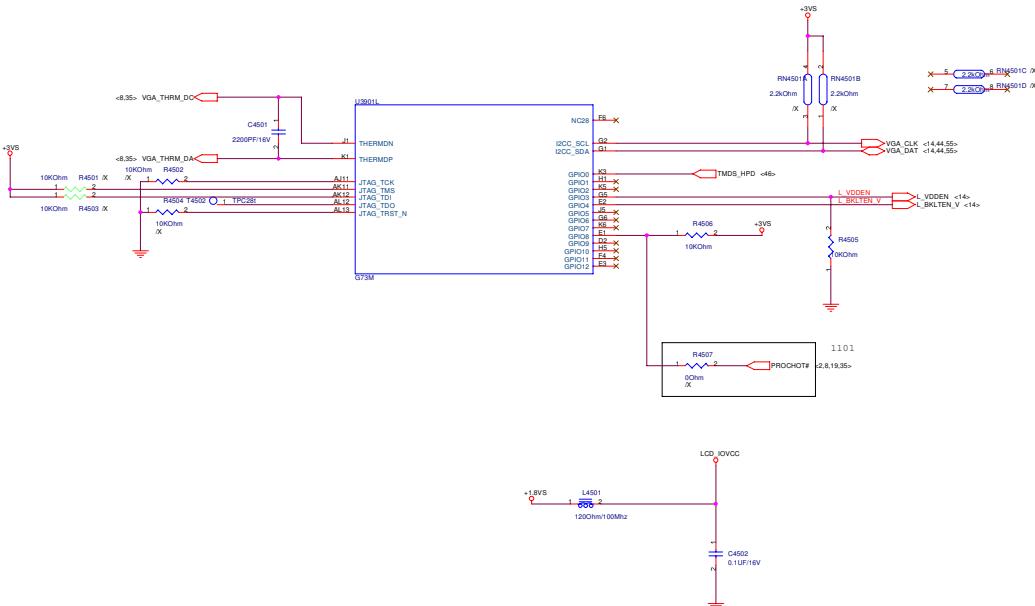


**ASUS** Title : G73M 4 DISPLAY  
ASUSTeCH Project Name : ATT  
Engineer : PENG XIAO  
Date : 08/01/2008 Rev : 2.0

<< Kennedy\_Zhang >>

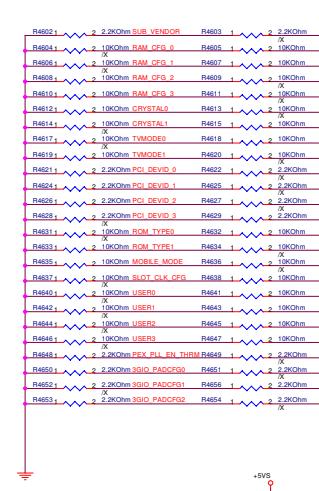
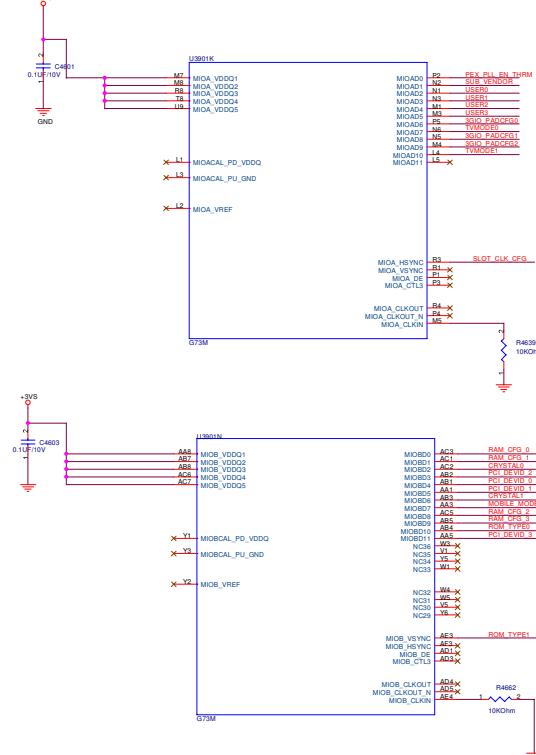


<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>





```

SUB_VENDOR   0:SYSTEM BIOS 1:ADAPTER
RAM_CFG[3..0]          0001:8*16*16 DDR2 SAMSUNG

RAM_CFG[3]      0: Full width of the frame buffer
                1: Half width of the frame buffer

CRYSTAL[1:0]     00 13.5MHz
                  01 14.318MHz
                  10 27.0MHz* (Default)
                  11 Reserved

TVMODE[1:0]      00 SECAM
                  01 NTSC (Default)
                  10 PAL
                  11 VGA

PCI_DEVID[3..0]   1 0 100 : GT3M
                  0 1 1 1 : GT3M-V

ROMTYPE[1:0]     00 Parallel
                  01 Serial (Default)
                  10 Reserved
                  11 LPC

ROM_TYPE        0 :PARALLEL 1: SERIAL
MOBILE_MODE     0 Enable (Default)
SLOT_CLK_CFG

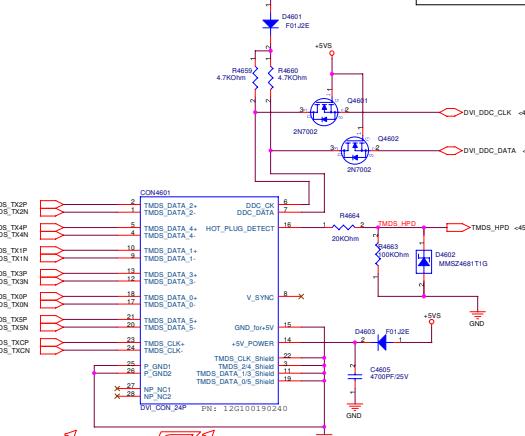
1 GPU and MCH share a common reference clock
  (Default)

USER[3..0]       1101 WXGA 1280x800 -/- 

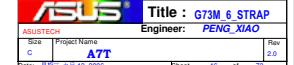
PEX_PLL_EN_Thrm  0 Enable (Default)
                  1 Disable

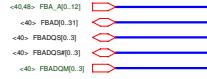
3GIO_PADCFC[2:0] 001 Mobile2 for GTx, NV42

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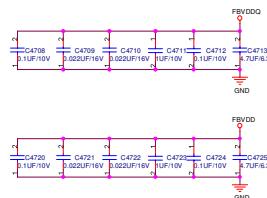
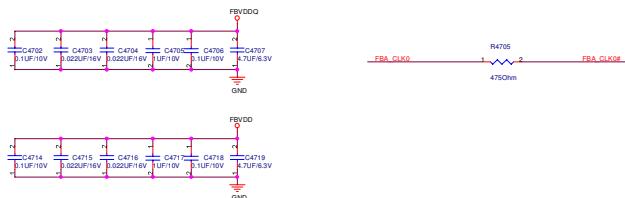
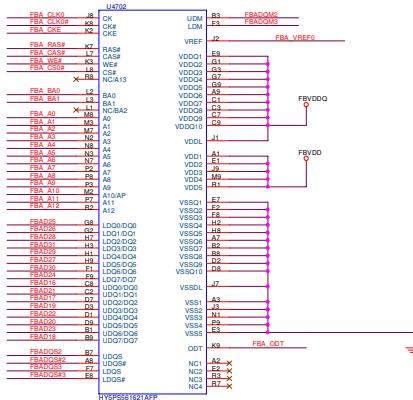
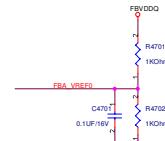
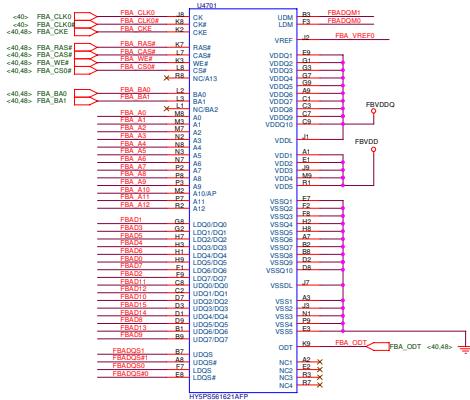


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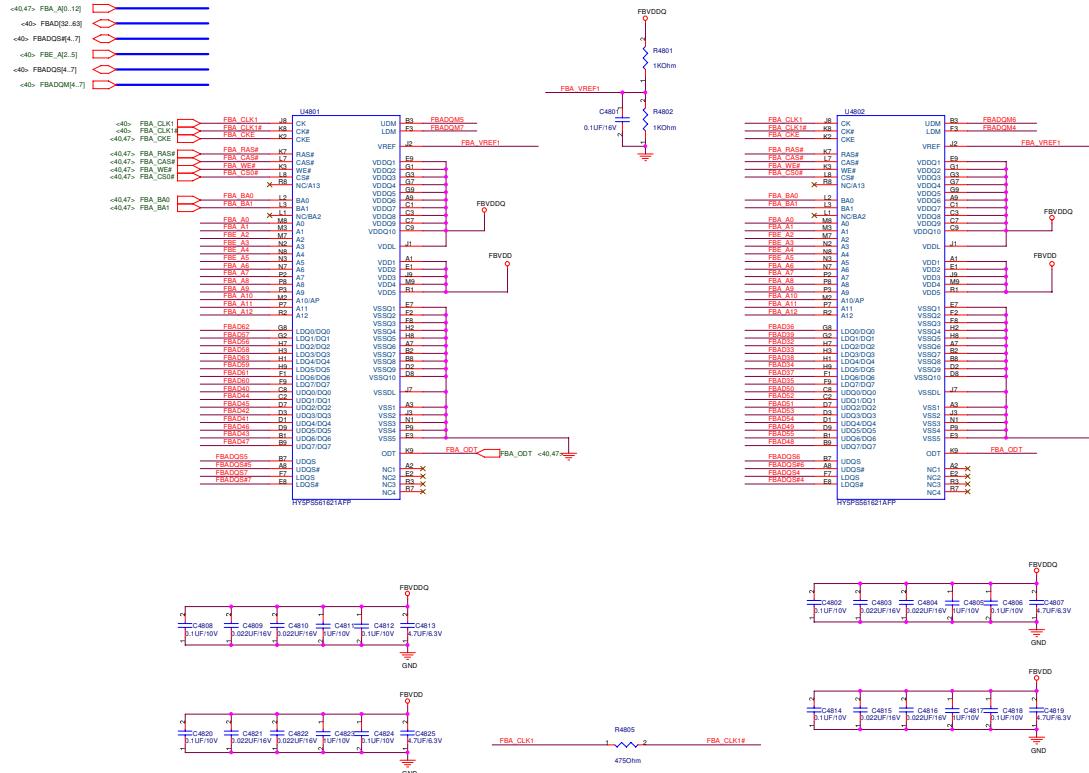


change BOM

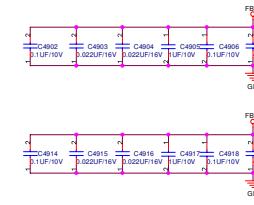
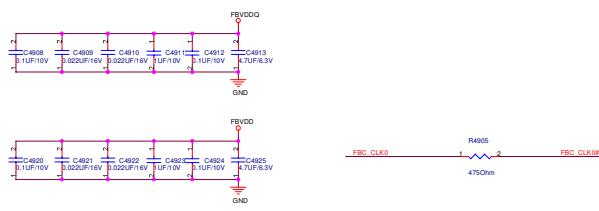
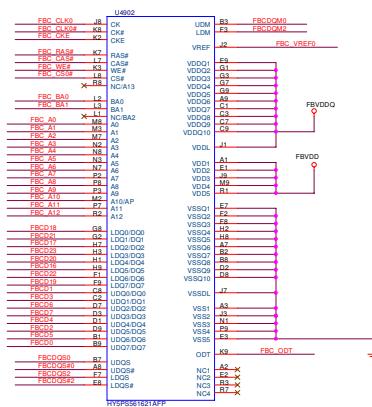
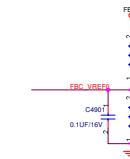
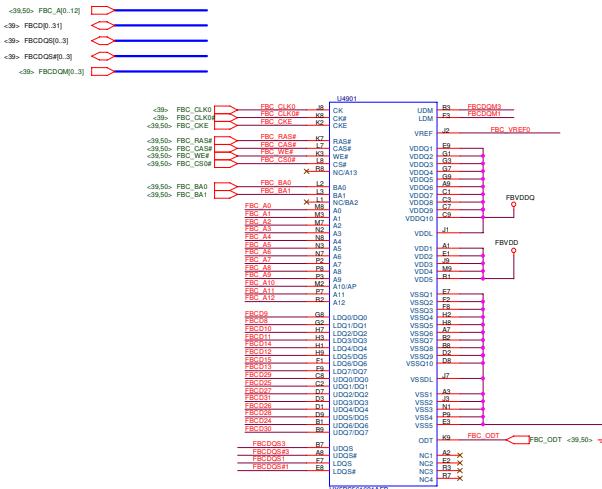


<< Kennedy\_Zhang >>

 Title : G73M\_VRAM1  
 ASUSTECH Engineer: PENG\_XIAO  
 Size Project Name Rev  
 C A7T 2.0  
 Date: 08-01-08 - Page: 17 / 47



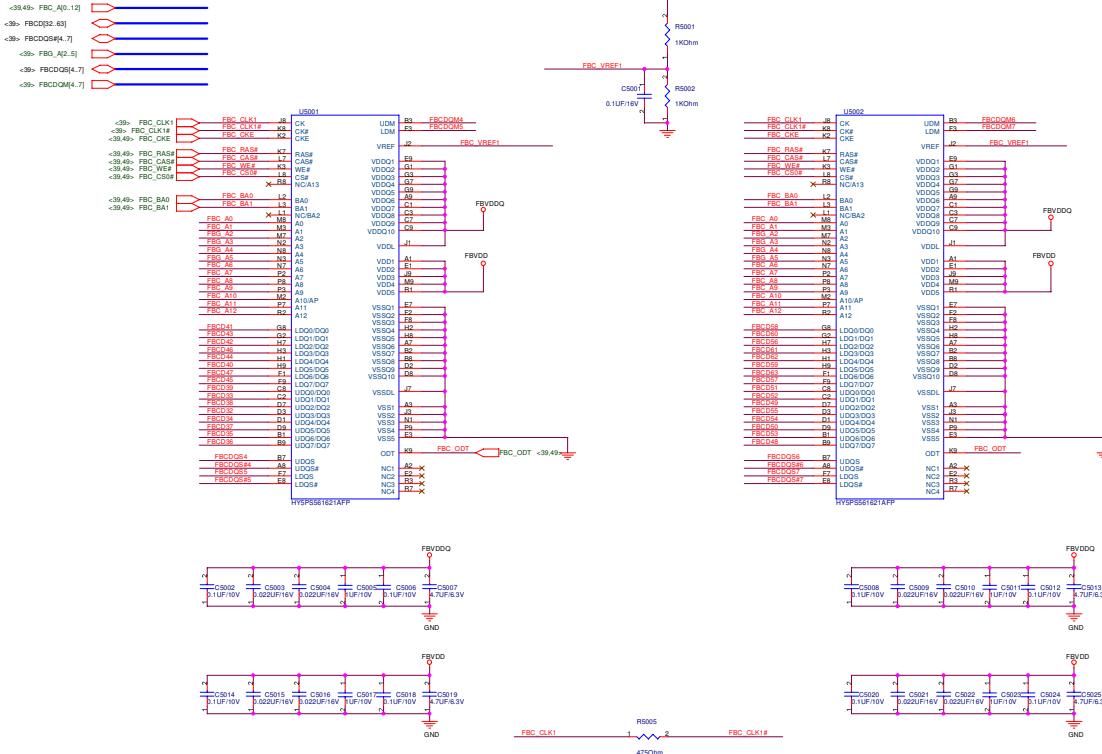
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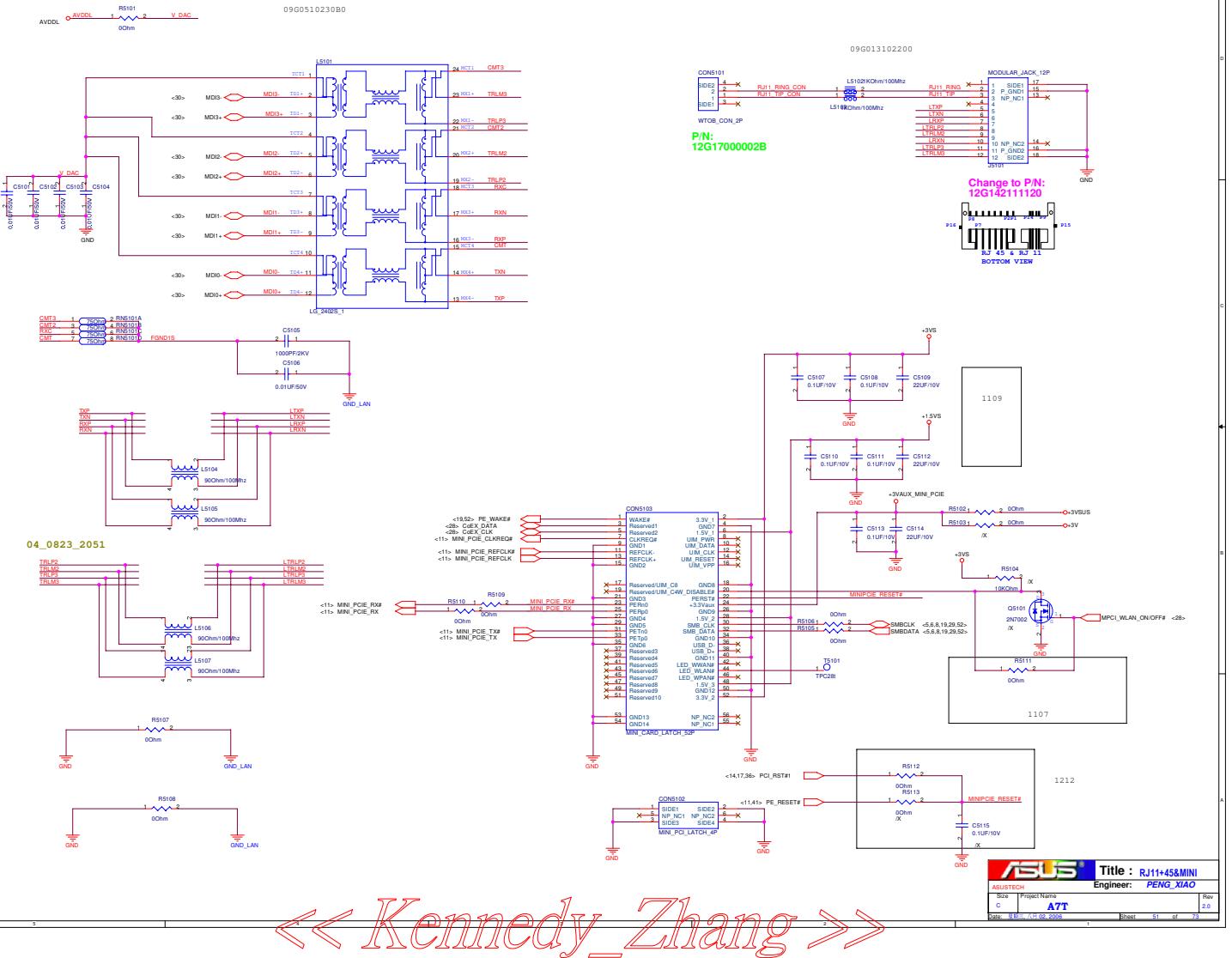
<< Kennedy\_Zhang >>

The image shows the ASUS logo at the top left. To its right is a table with the following data:

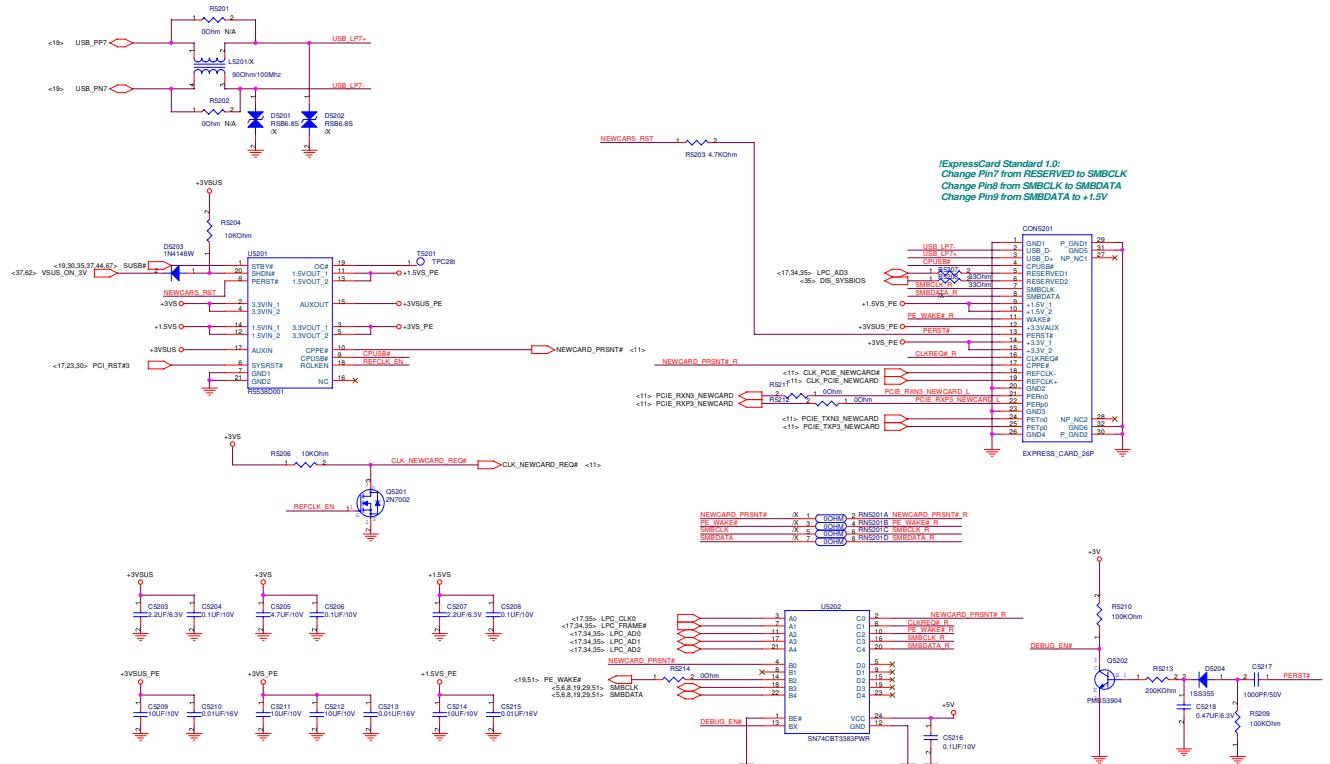
ASUSTECH		Title : G73M_VRAM3
Size C	Project Name ATT	Engineer: PENG_XIAO
		Rev 2.0



<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>



<< Kennedy\_Zhang >>

**ASUS** Title : NEWCARD  
 ASUSTEK Project Name : ATT Engineer: echo\_xing  
 Date: 2008-04-04 2008 Sheet 52 of 79 Rev 2.0

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	A
CARD READER	AD17	1	C
1394	AD17	1	B
MINIPCI ( 802.11a/b/g )	AD19	3	B,C
MINIPCI ( TV )	AD18	0	A,D

Host	SM-Bus Device	SM-Bus Address	Device
MCP51	Voice DSP	1100000x ( C2H )	VP1010
MCP51	SO-DIMM 0	1010000x ( A0H )	DDR SOCKET1
MCP51	SO-DIMM 1	1010010x ( A4H )	DDR SOCKET2
MCP51	Thermal Sensor	0101110x ( 5CH )	ADT7463 (Optional)
PIC		1001001x ( 92H )	Charge IC
M38857		0001000x ( 10H )	KBC control IC
BQ2060		16H-17H	Battery sensor IC

MCP51 GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 1	INPUT	KB_SCI#			+3VS	
GPIO 2	INPUT	SIO_SMI#			+3VS	
GPIO 3	OUTPUT	BACK_OFF#	LOW	HIGH	Off	+3VS
GPIO 4	OUTPUT	FWH_WP#	LOW	LOW	Off	+3VS
GPIO 5	OUTPUT	802_LED_EN#	LOW	HIGH	Driven	+3VSUS
GPIO 6					+3VSUS	
GPIO 7	OUTPUT	BT_LED_EN#	LOW	HIGH	Driven	+3VSUS
GPIO 8					+3VSUS	
GPIO 9					+3VSUS	
GPIO 10					+3VSUS	
GPIO 11	OUTPUT	BT_ON#	LOW	LOW	Off	+3VS
GPIO 12	OUTPUT	WLAN_ON#	LOW	LOW	Off	+3VS
GPIO 13					+3VSUS	
GPIO 14					+3VSUS	
GPIO 15	INPUT	PROCHOT#	LOW	HIGH	Off	
GPIO 16					+3VSUS	
GPIO 17		LID#			+3VSUS	
GPIO 18		USB_OC#0			+3VSUS	
GPIO 19		USB_OC#1			+3VSUS	
GPIO 20		USB_OC#2			+3VSUS	
GPIO 21		USB_OC#3			+3VSUS	
GPIO 22		ACZ_SDIN0			+3VSUS	
GPIO 23		ACZ_SDIN1			+3VSUS	
GPIO 24					+3VSUS	
GPIO 25					+3VSUS	
GPIO 26					+3VSUS	
GPIO 27		SMB_CLK			+3VSUS	
GPIO 28		SMB_DATA			+3VSUS	
GPIO 29		SMB_ALERT#			+3VSUS	
GPIO 30		PCL_PME#			+3VSUS	
GPIO 31		SIO_PME#			+3VSUS	
GPIO 32		EXTSMI#			+3VSUS	
GPIO 33		R1#			+3VSUS	
GPIO 34		SUS_CLK	PULL-DOWN:Normal mode select			
GPIO 40					+3VSUS	
GPIO 41					+3VSUS	
GPIO 46	SPDIFO	PULL-HIGH:SIO_CLK select 24MHz			+3VS	
GPIO 47	INPUT	RF_OFF_SW#	LOW	HIGH	Off	+3VS
GPIO 61	INPUT	PANEL_ID0			Off	+3VS
GPIO 62	INPUT	PANEL_ID1			Off	+3VS

KBC GPIO	I/O Mode	Signal	Active	S0 Default	S3
P23(Pin 35)	OUTPUT	BAT_LEARN	HIGH	LOW	LOW
P22(Pin 36)	OUTPUT	KBC_P21	HIGH	LOW	LOW
P20(Pin 38)	OUTPUT	KBCRSM	HIGH	LOW	LOW
P42(Pin 23)	OUTPUT	WATCHDOG	HIGH	LOW	LOW
P43(Pin 22)	INPUT	LID_KBC#			
P44(Pin 21)					
P45(Pin 20)	OUTPUT	KB_GATEA20			
P46(Pin 19)	OUTPUT	KBSCL#			
P47(Pin 18)		PM_CLKRUN#			
P50(Pin 17)	INPUT	BAT_LL0W#_OC			
P51(Pin 16)	INPUT	KB_ID0			
P52(Pin 15)	INPUT	KB_ID1			
P53(Pin 14)	OUTPUT	CLR_DJ#	LOW	LOW	Driven
P54(Pin 13)	INPUT	BAT_SEL#			
P55(Pin 12)	INPUT	BAT1_IN#_OC			
P56(Pin 11)	OUTPUT	FAN_DAI(Optional)	Analog	Analog	Driven
P57(Pin 10)	OUTPUT	INVTER_DA	Analog	Analog	Driven
P67(Pin 74)	OUTPUT	DJ_LED#	LOW	HIGH	HIGH
P66(Pin 75)	INPUT	SWD1_EN#			
P65(Pin 76)	INPUT	CHG_FULL_OC			
P64(Pin 77)	INPUT	ACIN_OC			
P63(Pin 78)	INPUT	DISPT_SW#			
P62(Pin 79)	INPUT	P4GEAR_SW#			
P61(Pin 80)	INPUT	EMAIL_SW#			
P60(Pin 1)	INPUT	INTERNET_SW#			
P75(Pin 4)		KB_CLK			
P74(Pin 5)		MS_CLK			
P73(Pin 6)		TPAD_CLK			
P72(Pin 7)		KB_DAT			
P71(Pin 8)		MS_DAT			
P70(Pin 9)		TPAD_DAT			
P77(Pin 2)		SMC_BAT			
P76(Pin 3)		SMD_BAT			
P27(Pin 31)					
P26(Pin 32)	OUTPUT	NUM_LED#	LOW	Define	HIGH
P25(Pin 33)	OUTPUT	CAP_LED#	LOW	Define	HIGH
P24(Pin 34)	OUTPUT	SET_PLIRSTNS#	LOW		
P40(Pin 27)	OUTPUT	EXT_SMI			
P41(Pin 26)	OUTPUT	EMAIL_LED#	LOW	HIGH	HIGH

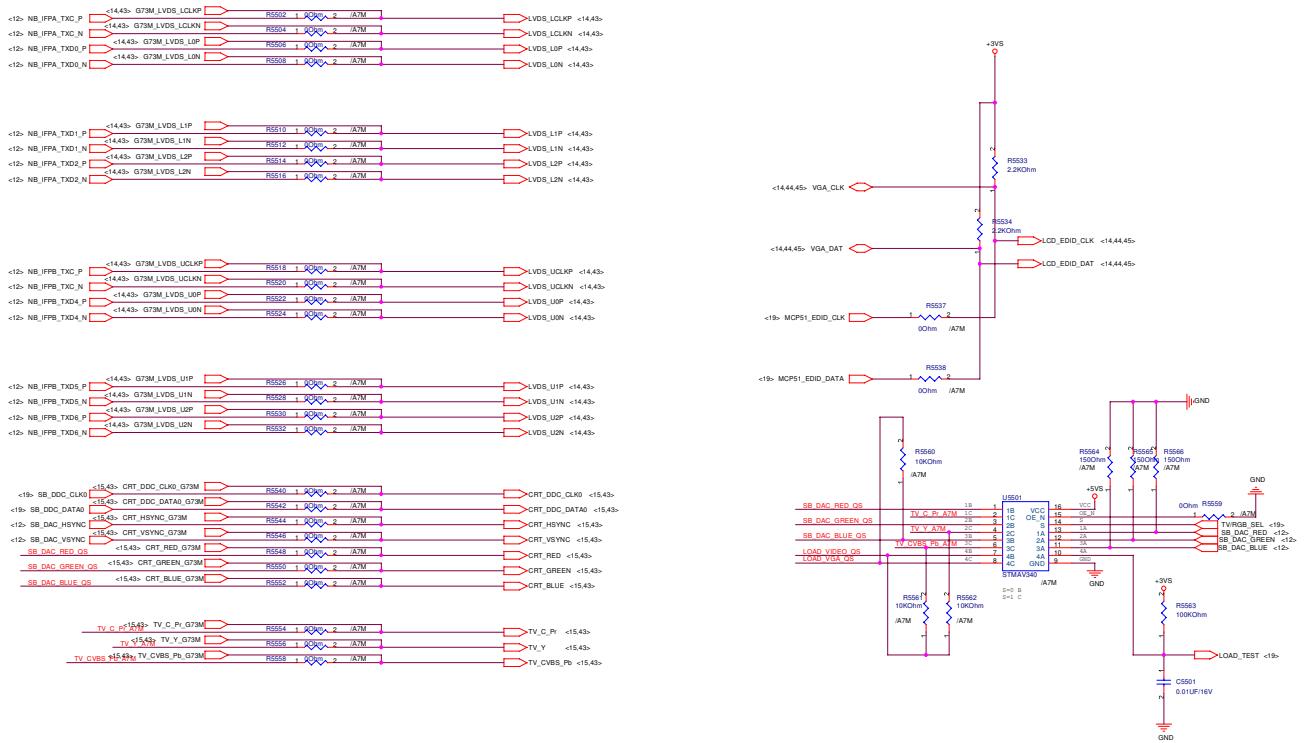
MCP51 GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 16	OUTPUT	DSP_SH1_EN	HIGH	HIGH	Off	+5VS
GPIO 53	INPUT	SUSC#	LOW	HIGH	H/L	+5VS
GPIO 45	INPUT	SUSB#	LOW	HIGH	LOW	+5VS
GPIO 11	INPUT	PROCHOT#	LOW	HIGH	Off	+5VS

<< Kennedy\_Zhang >>

Rev	Date	Description

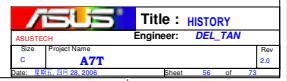
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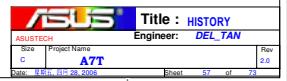


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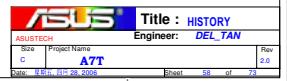
**ASUS** Title : LVDS SWITCH  
ASUSTECH Engineer: DEL\_TAN  
SD4 Project Name: ATT Date: 08/01/2008 Rev: 2.0



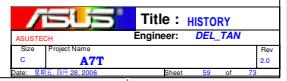
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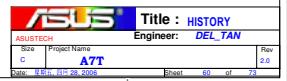
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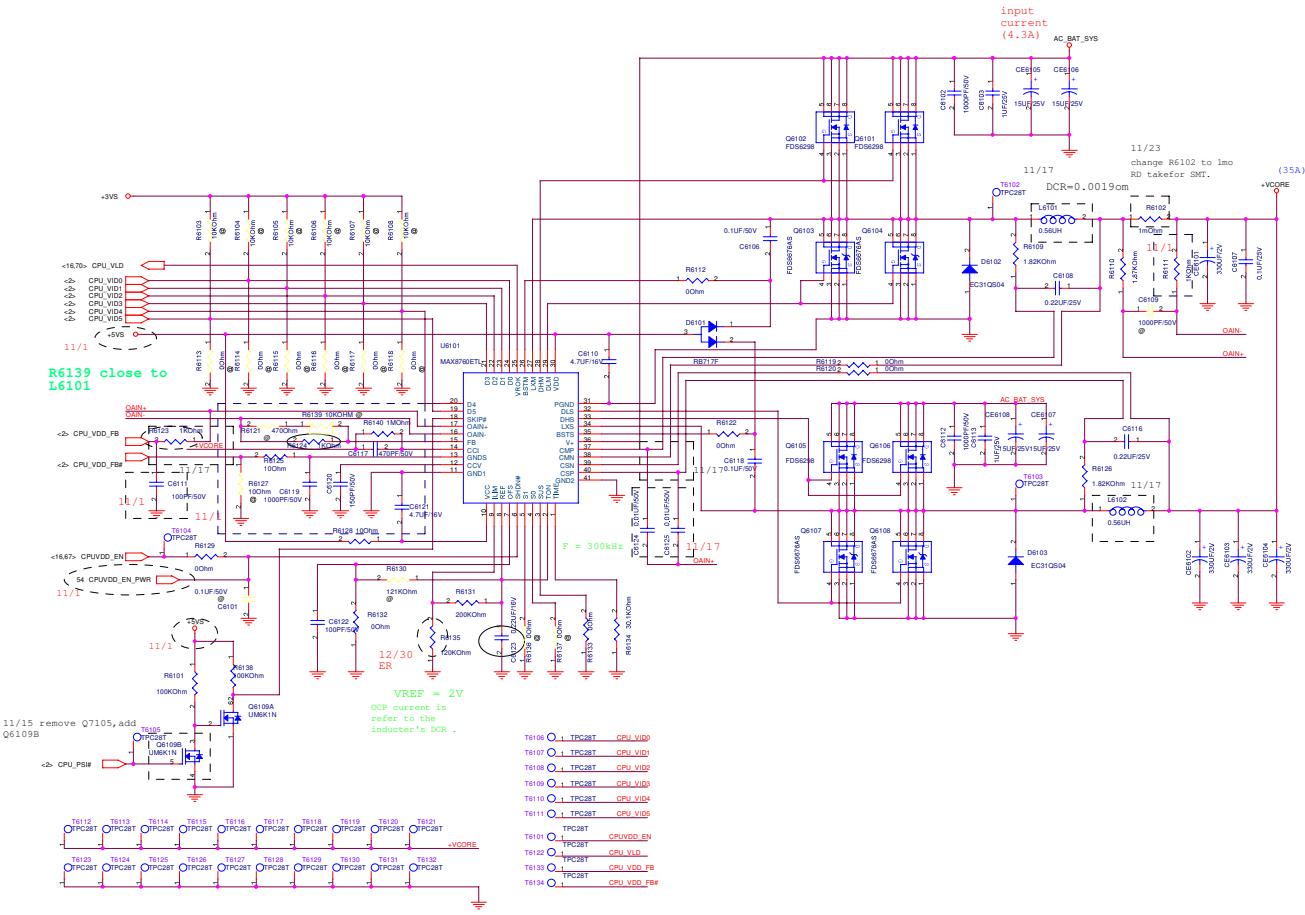
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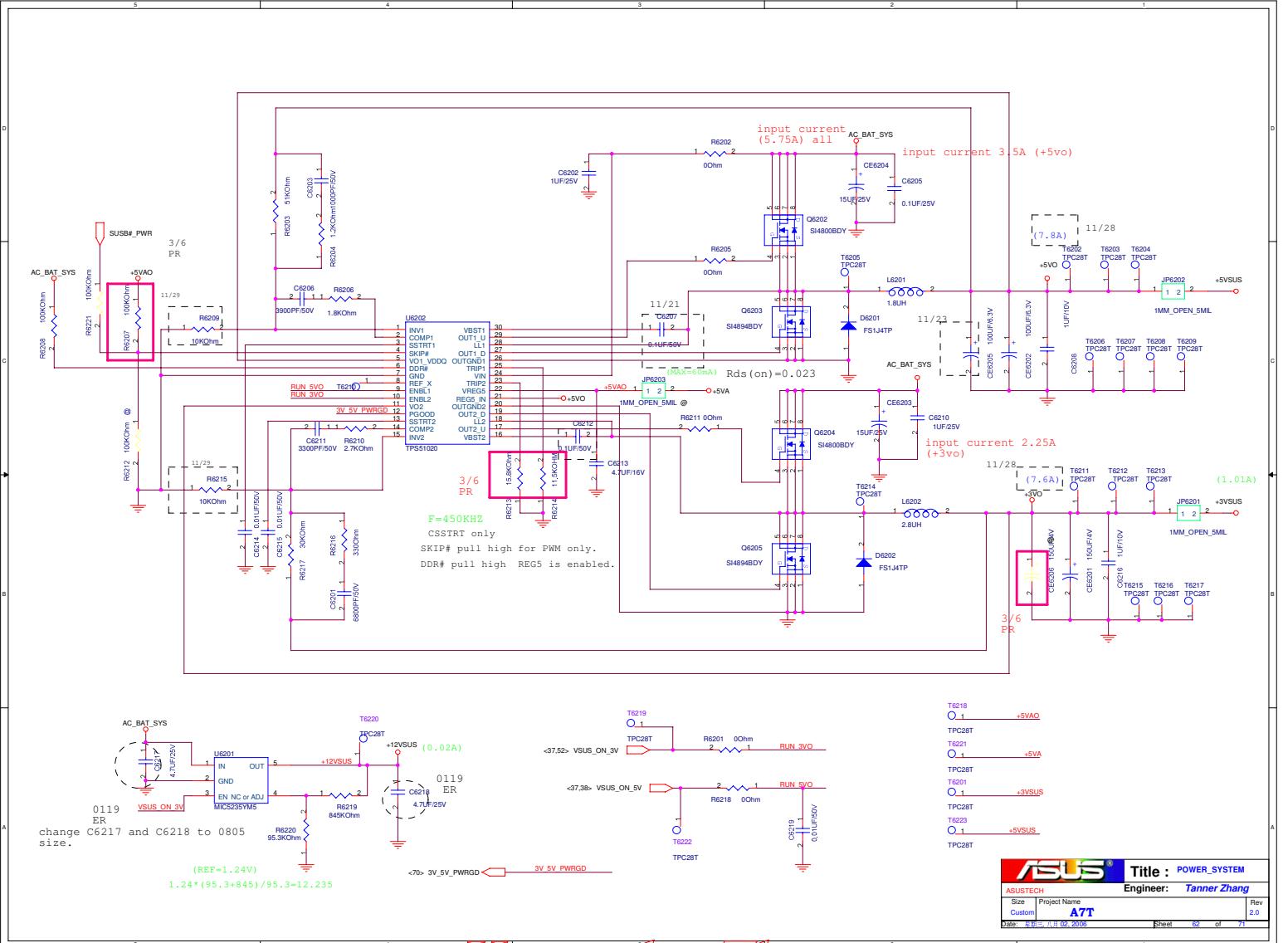


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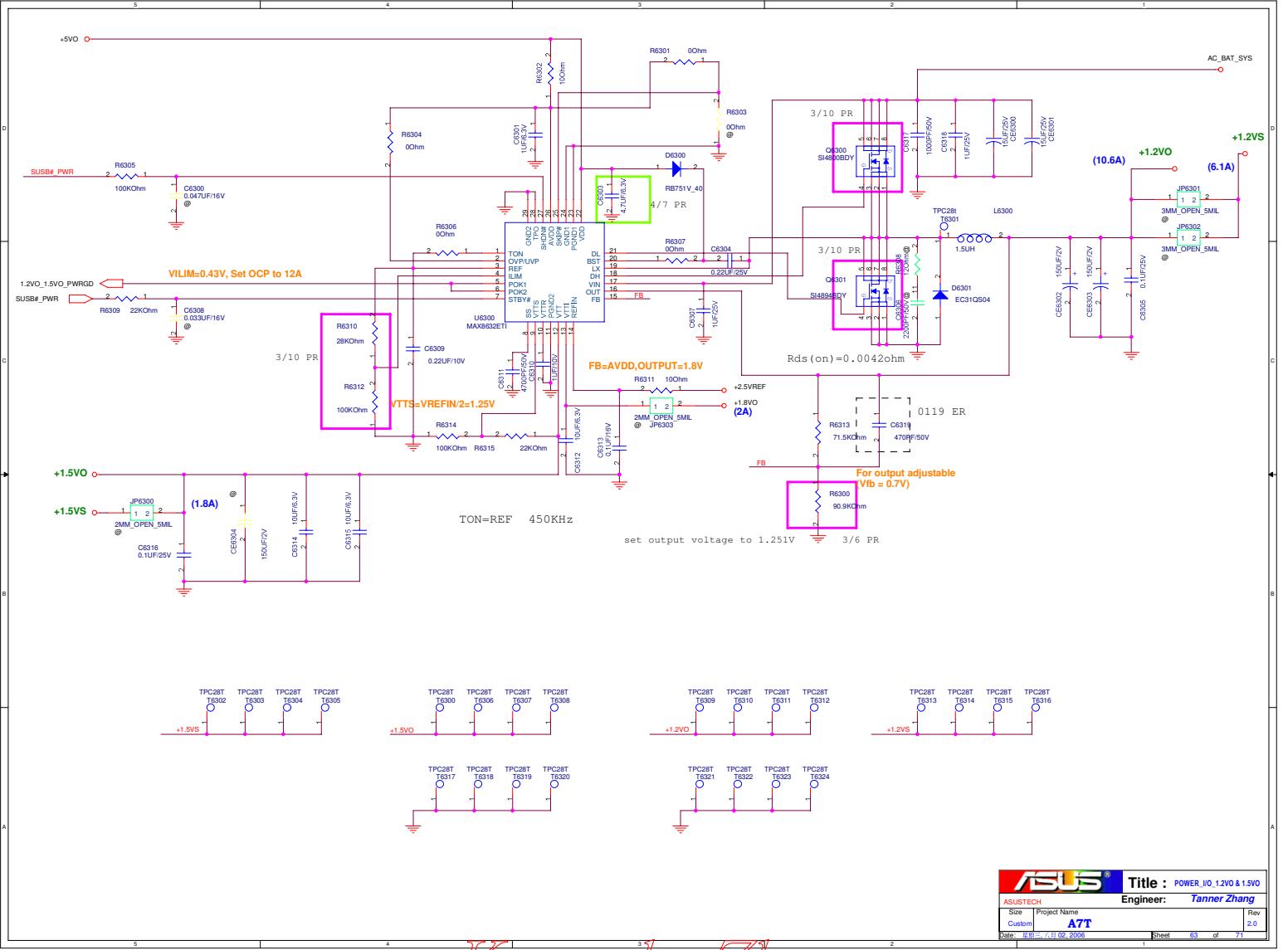


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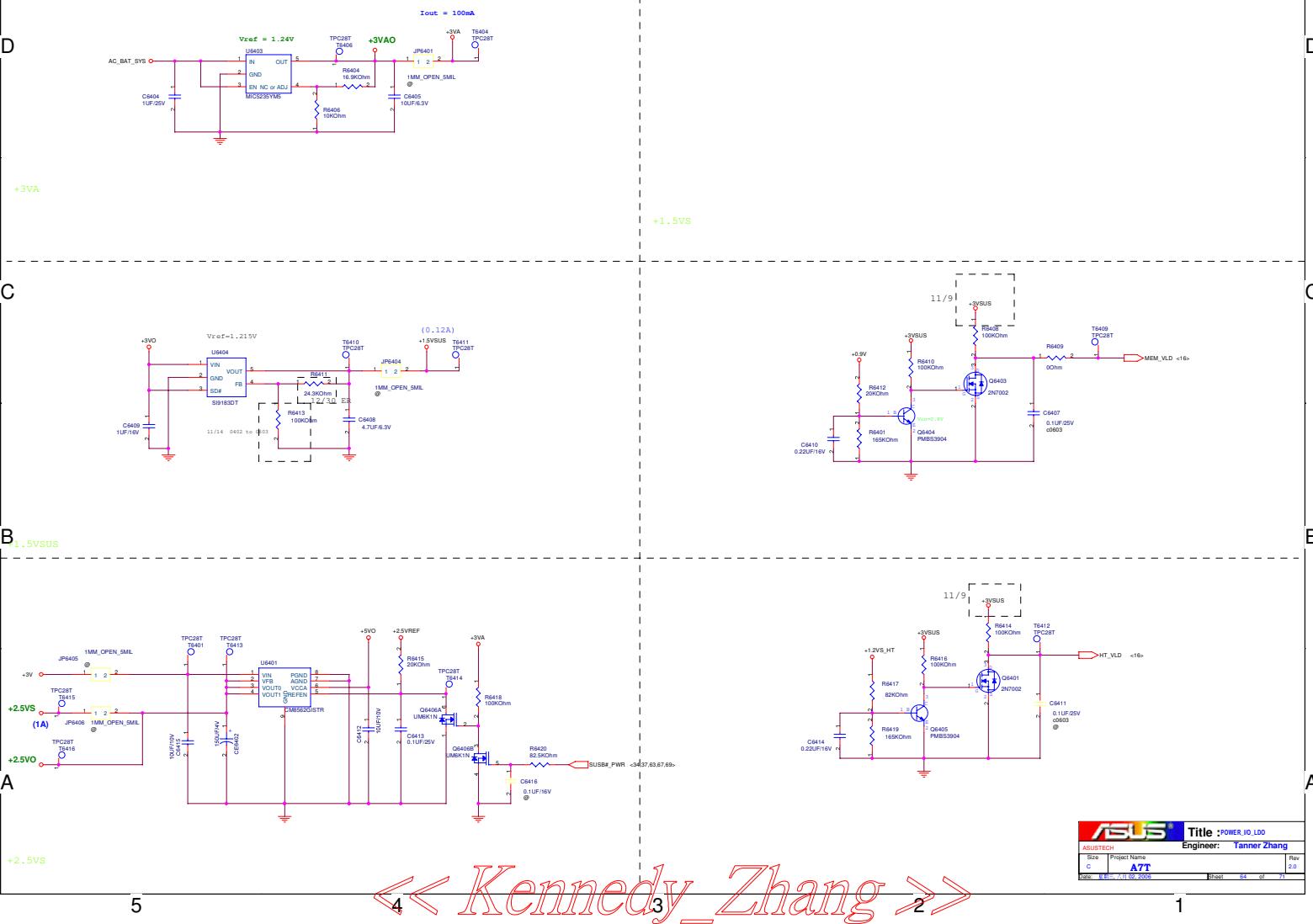


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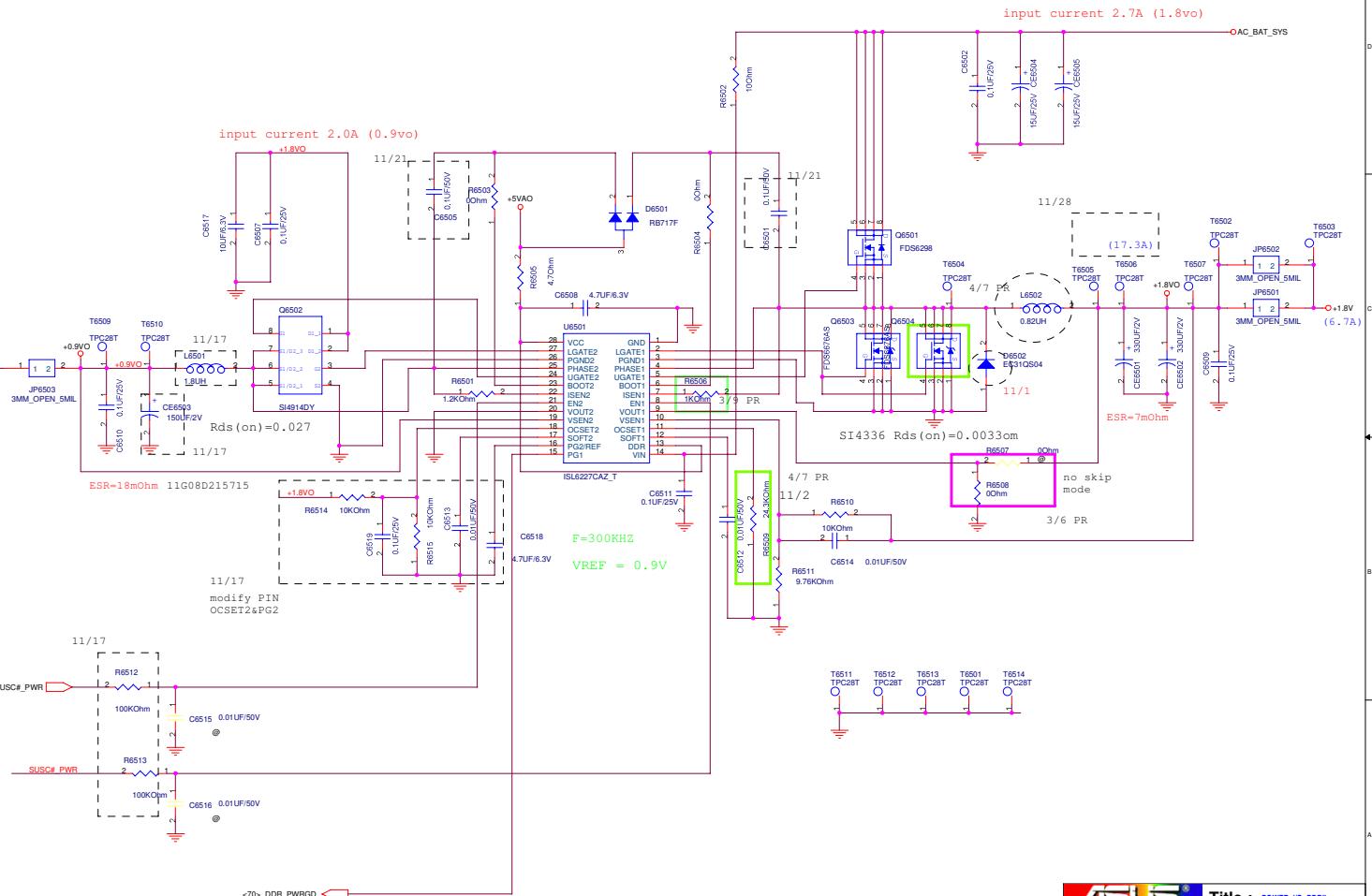


ASUS		Title : POWER IO_1.2VO & 1.5VO
ASUSTECH		Engineer: Tanner Zhang
Size	Project Name	Rev
Custom	A7T	2.0
Date: 08-01-02, 2006	Sheet 63 of 71	

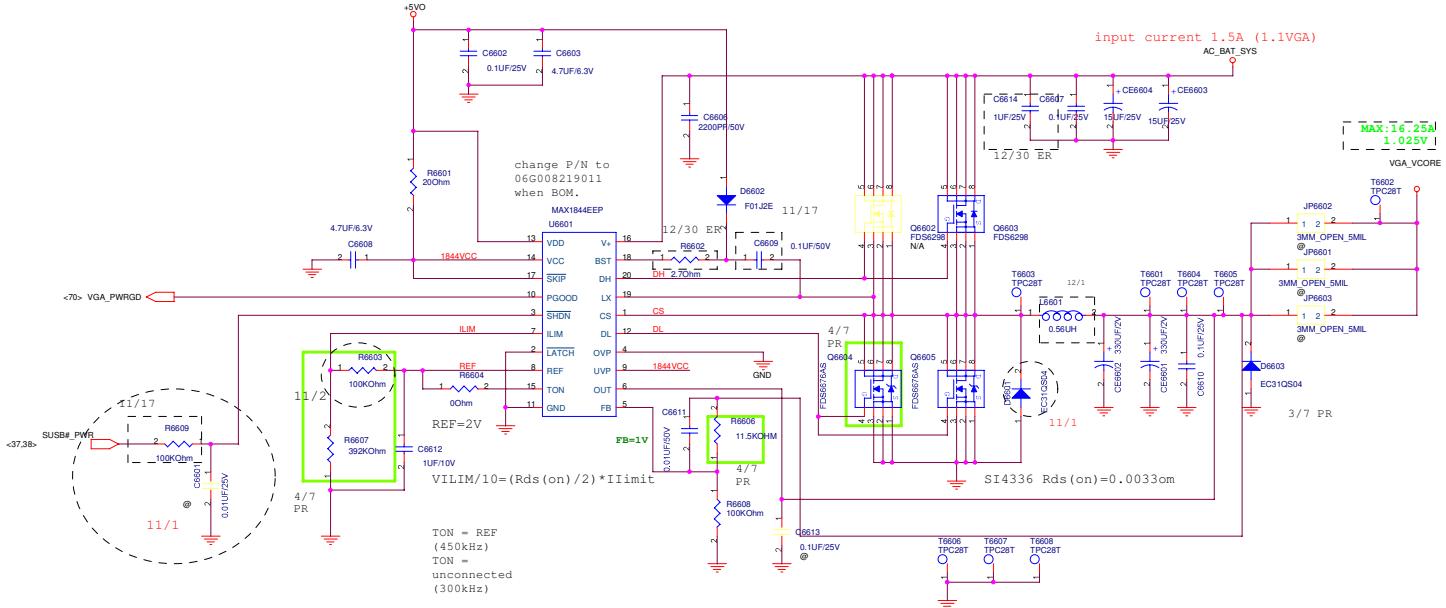
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4 3 2 << Kennedy\_Zhang >>

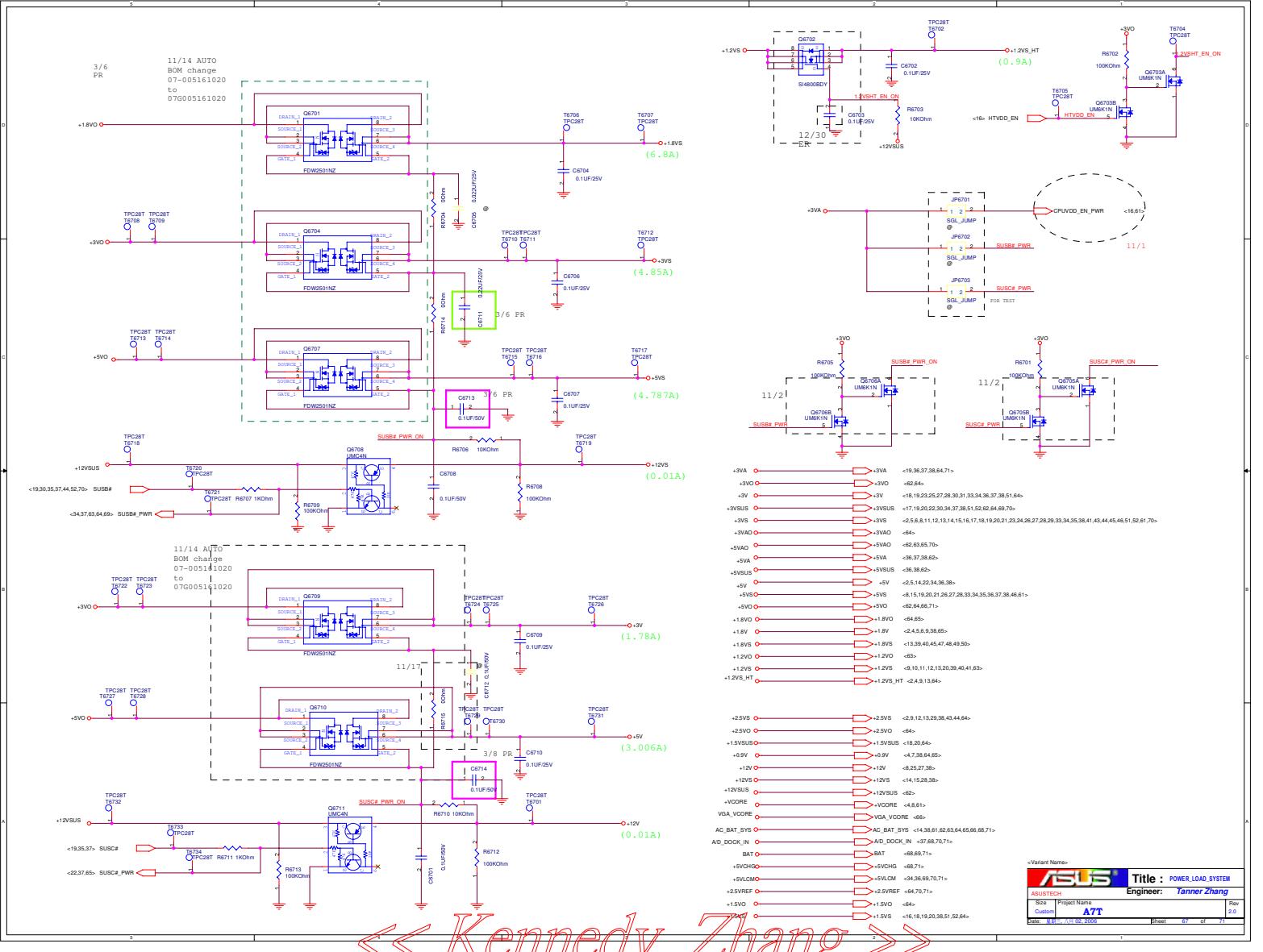


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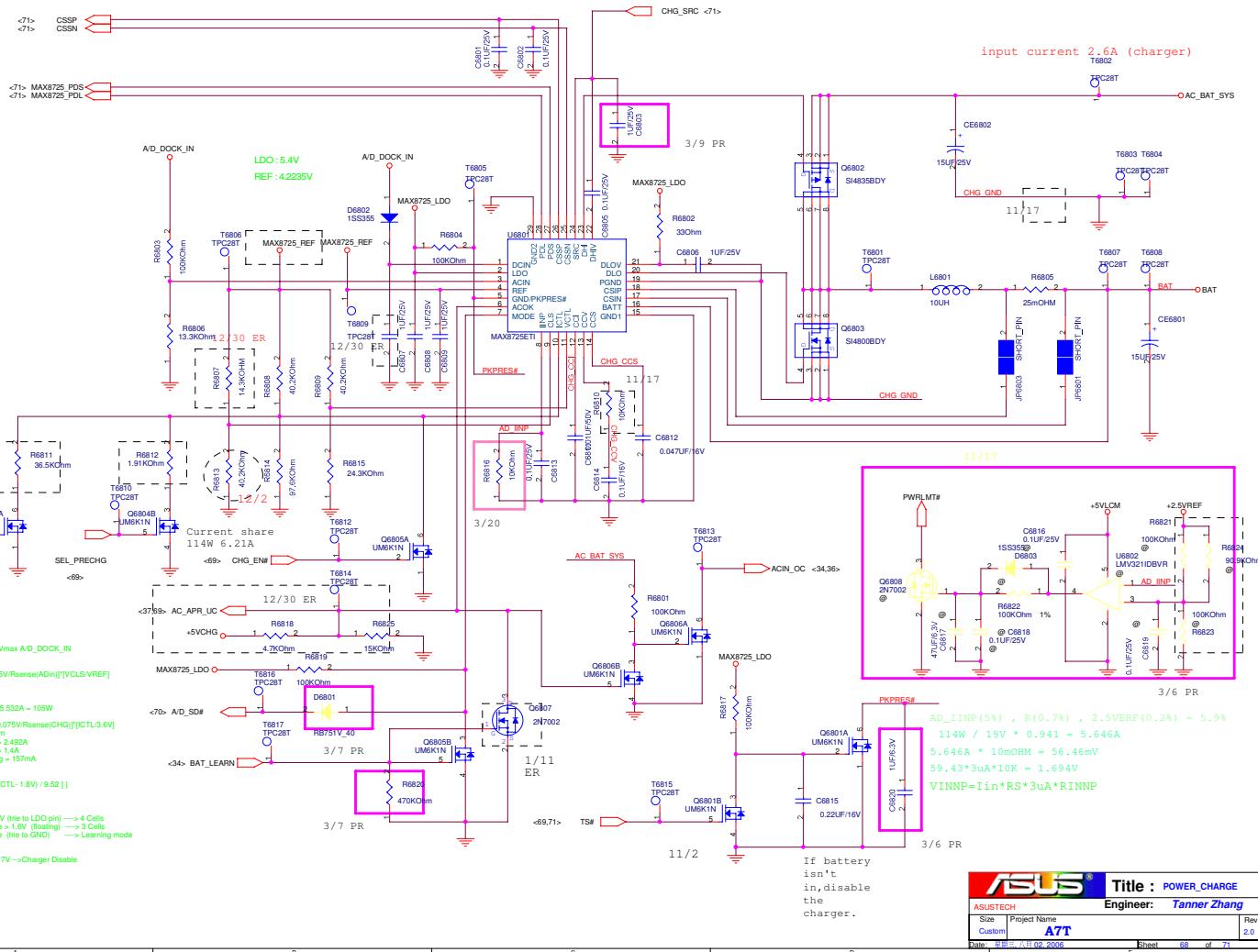


<Variant Name>  
 Title : POWER\_VGACORE  
 ASUSTek Engineer: Tanner Zhang  
 Size: Project Name: A7T  
 Custom: Date: 五月 02, 2006 Sheet 66 of 71  
 R 21

<< Kennedy\_Zhang >>



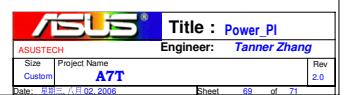
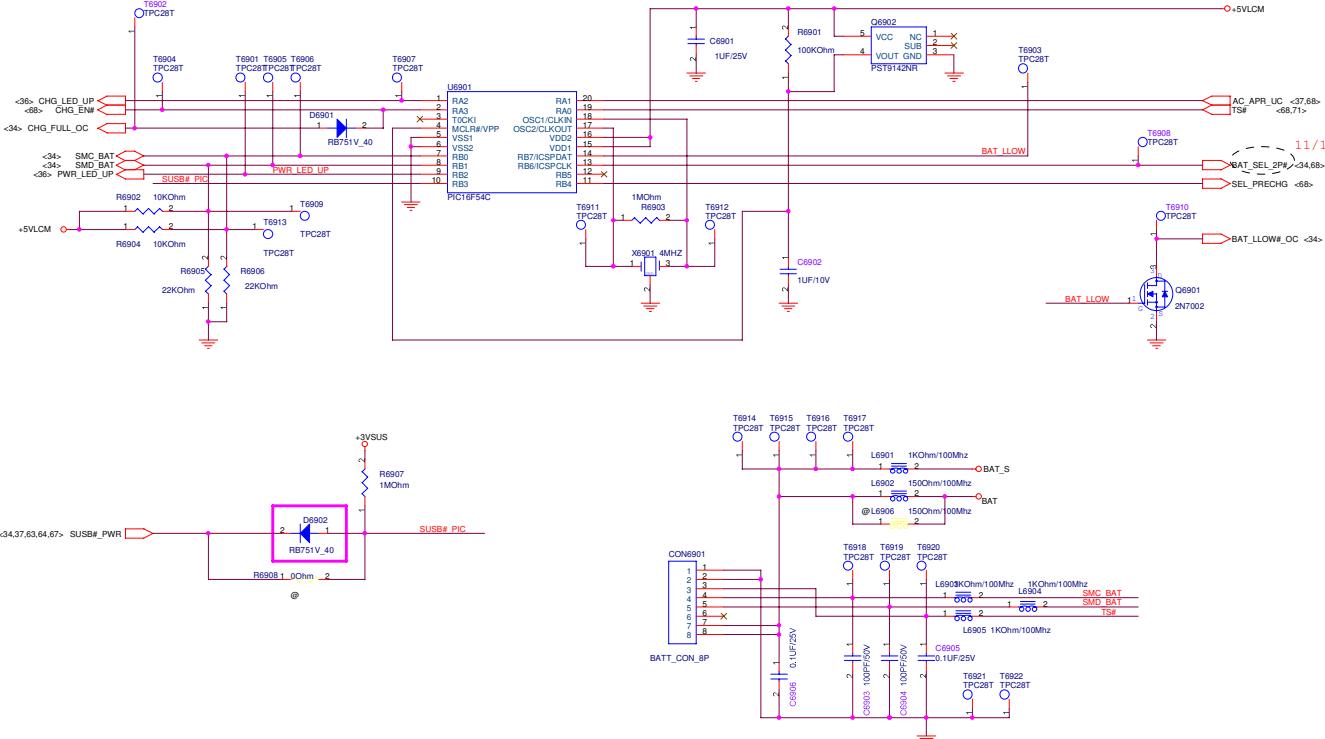
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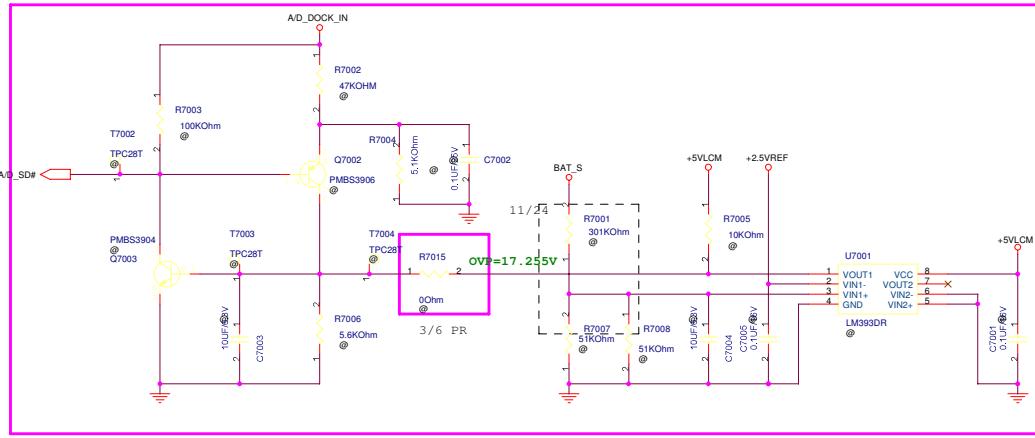
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<b>ASUS</b>		<b>Title :</b> POWER_CHARGE
<b>ASUSTECH</b>		<b>Engineer:</b> Tanner Zhang
Size	Project Name	Rev
Custom	A7T	2.0

Date: 8/26-01/02/2009 Sheet: 68 of 71

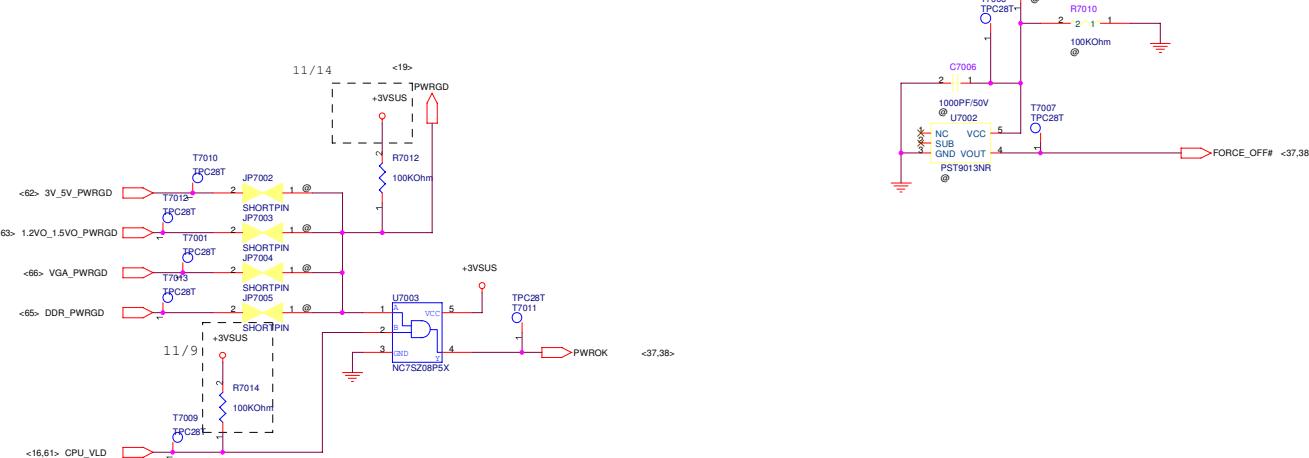


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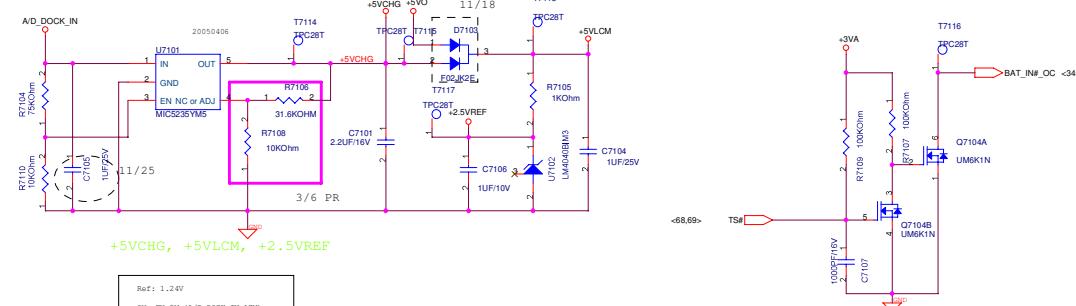
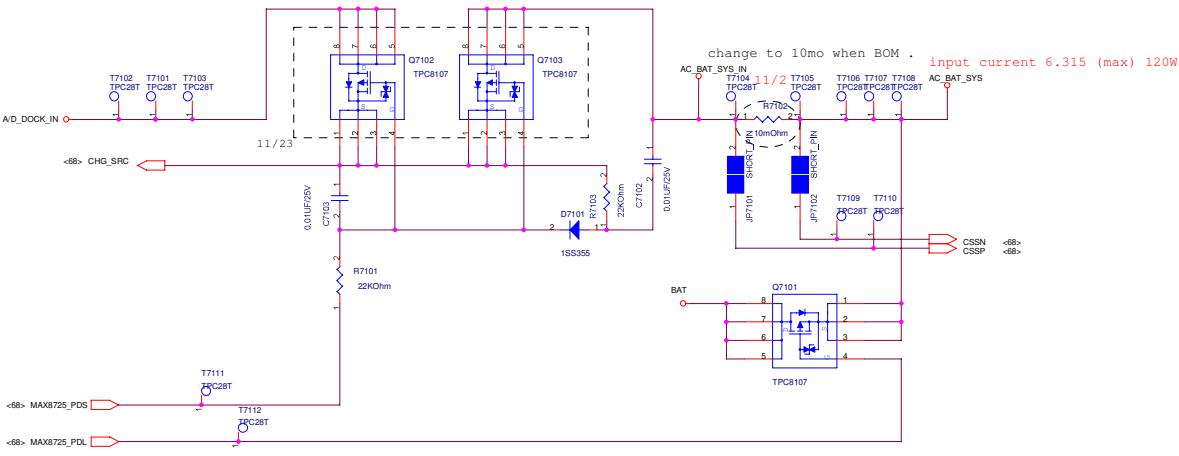
3/7 PR

#### **THERMAL PROTECTION**



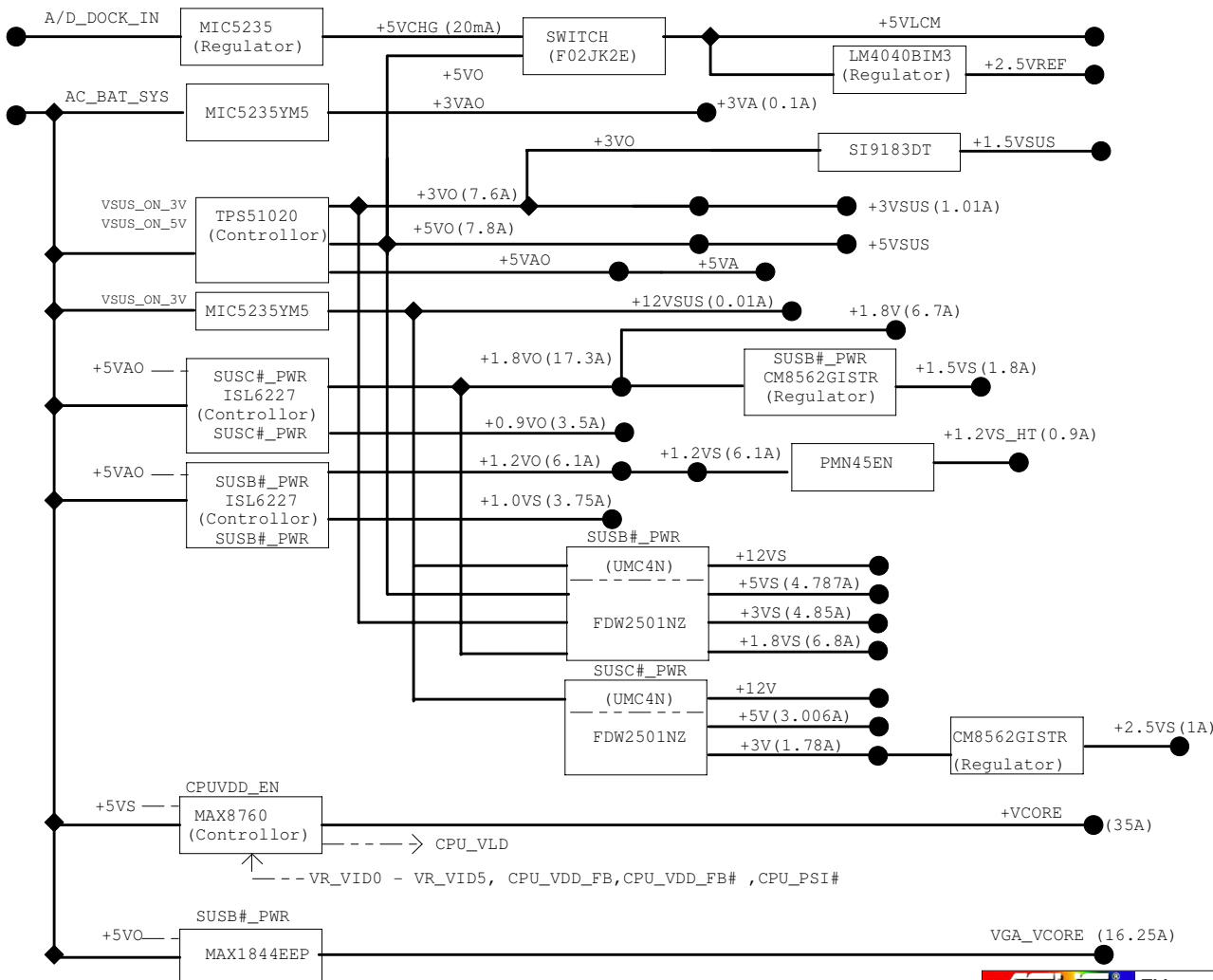
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ASUS Title : POWER SWITCH 5VLC  
 ASUSTECH Engineer: *Tanner Zhang*  
 Size Project Name Rev  
 Custom A7T 2.0  
 Date: 08月 2006 Sheet 71 of 71



<< Kennedy\_Zhang >>



